PRELIMINARY

March 28, 2014

YDA184(D-820Di) Evaluation Board

Control Software

User Manual

1. Function Description

D-820Di Control Software is the application which controls the function of D-820Di. Volume control, DRC control, etc. can be operated by accessing the built-in register of D-820Di through USB I/F.

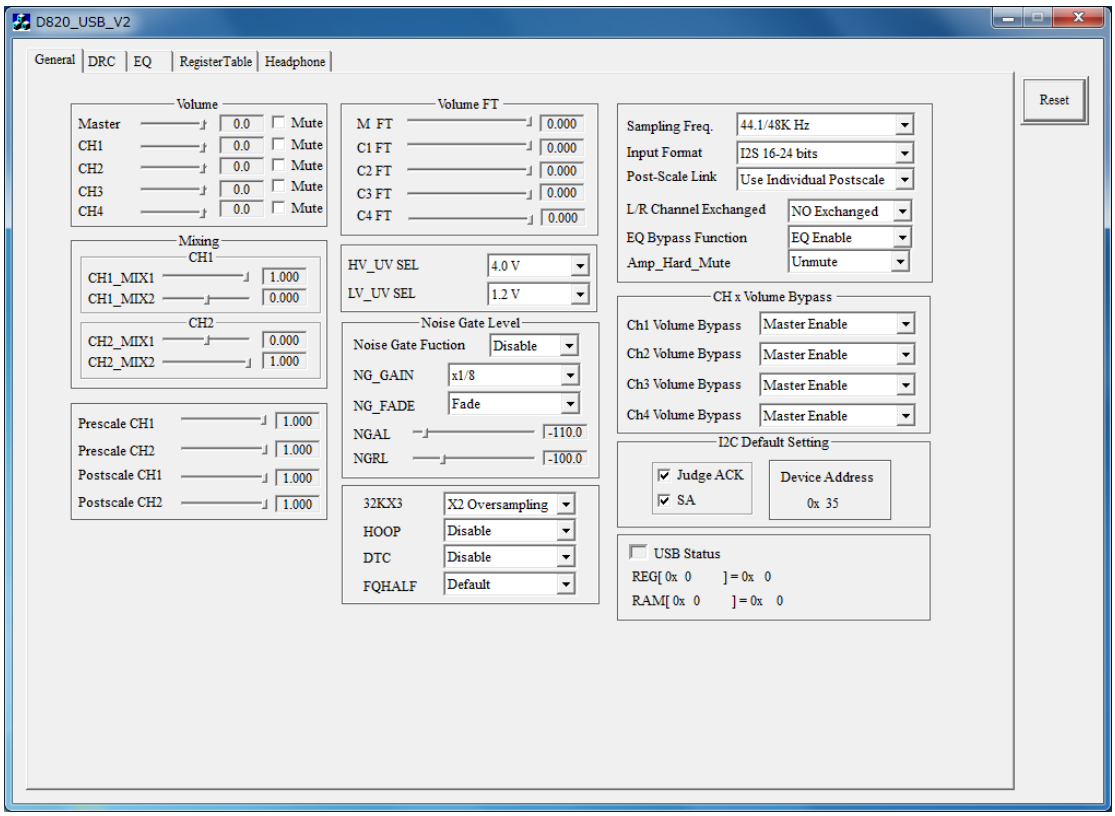
2. Procedure

(1) Copy "D820 Di_USB_V2.2.exe" and "UsbToI2cDll.dll" to the same folder on PC.

(2) D-820Di evaluation board is connected to PC with an attached USB cable.

(3) D-820Di evaluation board is power on.

(4) "D820 Di_USB_V2.2.exe" is started. The following GUI is displayed.



The control is divided into 5 pages: General, DRC, EQ, Register Table, and Headphone. In each page, each field is enclosed by a solid box. Each solid box will be described in this manual, from top to bottom and from left to right order.

Each page has a RESET button on the top right corner. When this button is pressed, registers in all pages will be reset to the default values.

On the General and DRC pages, the register that is adjusted will be instantly reflected in the REG[0x0] = 0x0 field.

The following four GUI selection methods are defined:

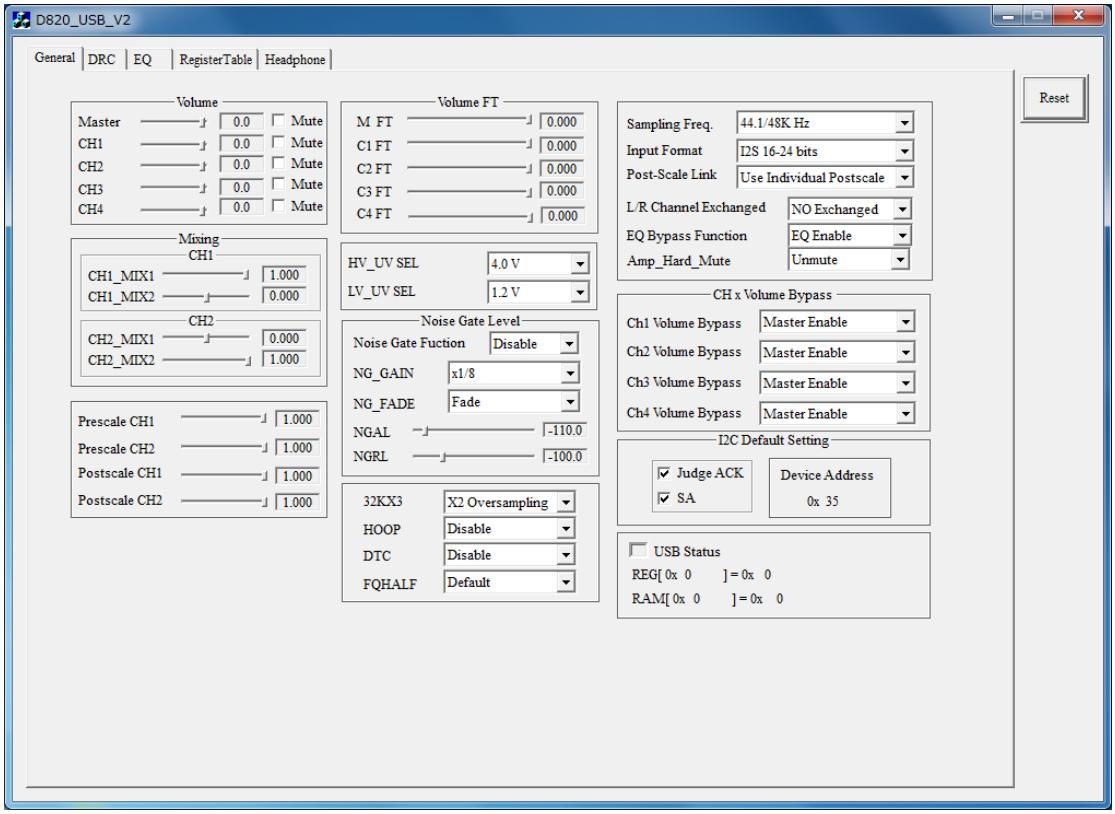
Check box: when this box is checked, a specific function is selected.

Slider: when a range of value is to be selected, sliding this bar.

Combo box: for multiple selections.

Edit box: numerical value can be entered here (in HEX format)

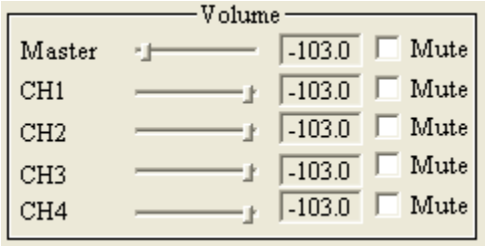
3. "General" Page



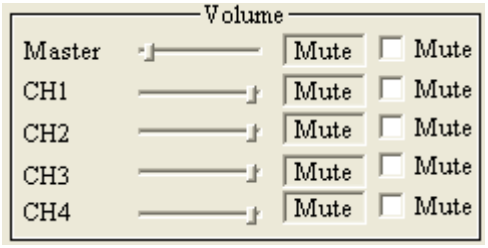
3.1 Volume Adjustment

Volume control consists of 2 parts: master and channel volume control. Each part ranges from -103dB to 6dB with .5dB increment. When Master Volume Bypass is unchecked as described in 2.23, the net volume for each channel shown in the above box (CH1, CH2, CH3 and CH4) is the sum of master and channel volume control. Otherwise, the net volume is determined by each channel volume, e.g., Master volume control is bypassed.

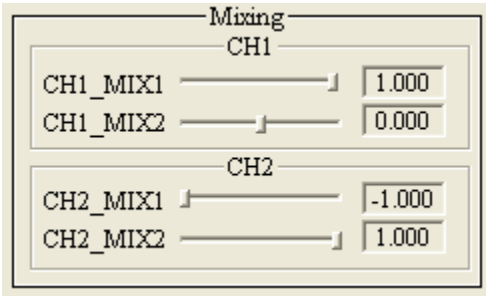
A channel is effectively muted when the net volume is below -103dB, being equivalent to checking the mute box. For the example shown below, Master is set to -103dB, while each channel is set to 0dB, making the volume of each channel set to -103dB.



When each channel's slide bar is moved slightly below 0dB, then each channel is muted, as shown in the following example.



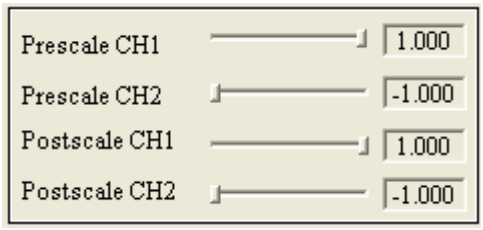
3.2 Audio Mixing



Audio mixing refers to the function of mixing channel 1 and 2 audio inputs to generate channel 1 and 2 audio outputs. Audio mixing can be additive or subtractive. The mixing range is adjustable by sliding the bar between +.9999 to -1.

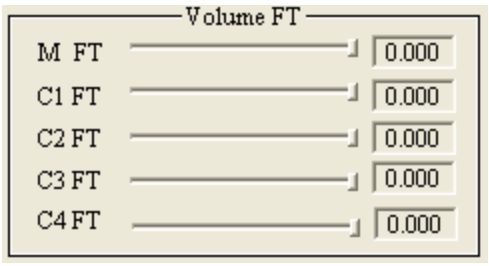
In the mixing checking box under CH1, CH1_MIX1 is the channel 1 mixing proportion to generate channel 1 output, while CH1_MIX2 is the channel 2 mixing proportion to generate channel 1 output. In the mixing checking box under CH2, CH2_MIX1 is the channel 1 mixing proportion to generate channel 2 output, while CH2_MIX2 is the channel 2 mixing proportion to generate channel 2 output.

3.3 Channel Pre and Post Scaling



Prescale is a programmable gain of CH1 and CH2 before any audio processing, while Postscale is a programmable gain of CH1 and CH2 after audio processing. Note the range of scaling is between +.9999 to -1.

3.4 Volume Fine Tune (VFT)



Note that in 2.1, each volume adjustment step is .5dB. When finer volume adjustment is desired, this box specifies the volume fine tune steps with .125dB/step for each channel. 4 selections are provided: 0, -0.125, -0.25, and -0.375dB.

M FT, C1 FT, C2 FT, C3 FT , and C4 FT are applied to Master, CH1, CH2, CH3 and CH4 respectively. For example, if in 2.1, CH1 is selected as -2dB, while in 2.4, CH1 VFT is selected as -0.375dB. Then the net CH1 volume adjustment is -2.375dB.

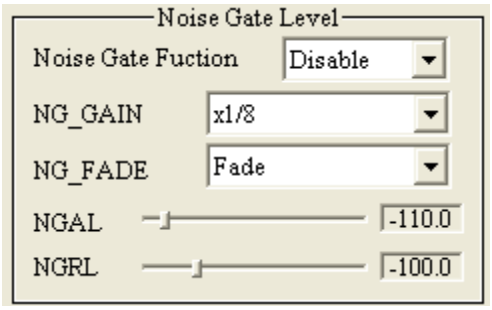
3.5 High Voltage (HV) Under-Voltage (UV) Protection

D820 has a High Voltage Under-Voltage Protection mechanism. When the high voltage that is applied to the output stage driver drops to a preset value (HV UV detect level), a signal will be generated to trigger the PWM output fade-out function, preventing the annoying pop noise from being generated. Five levels can be selected: 4V (default), 7V, 9V, 12V, and 15V.

3.6 Low Voltage (LV) Under-Voltage (UV) Protection

D820 has a Low Voltage Under-Voltage Protection mechanism. When the low voltage that is applied to the digital part drops to a preset value (LV UV Detect Level), a signal will be generated to trigger the PWM output fade-out function, preventing the annoying pop noise from being generated. Two levels can be selected: 1.2V (default) or 1.4V,

3.7 Noise gate selection



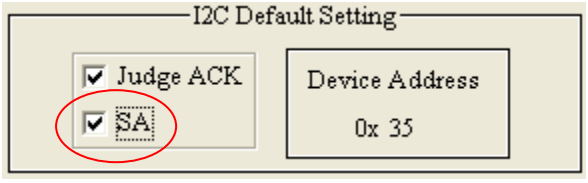
When the Noise Gate function is enabled, D820 will suppress very small input signal further to minimize the output audio noise. In other words, for any audio input signal, when it is less than NGAL, it will be treated as a noise, and its power is further reduced by NG_GAIN; Otherwise the reduced by NG_GAIN signal was large than NGRL, the reduced will be release. For instance, in the above selection, when the input signal is less than -110dB, D820 will reduce the signal to 1/8 of the original power. NGAL and NGRL were programmed by user, while NG_GAIN has 4 values to select: 1/8, 1/4, 1/2, and Mute.

3.8 Communication Interface

In order for the system host CPU to program these on-chip registers to fully utilize D820's flexibility, the industrial standard I^2C interface is used as the control channel between CPU (I^2C master) and D820 (I^2C slave device).

Each I^2C slave device shall have a unique 7-bit address (device address) for the CPU to identify for communication. In D820, 6 out of 7 device address bits are fixed (0 1 1 0 SA 0 1) inside the chip, while the one bit is defined by one pin, SA, allowing up to two different I^2C slave devices connected on the same I^2C bus within the system.

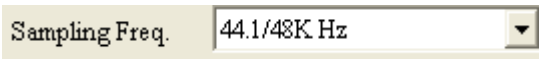
If there are multiple D820 chips on the same I^2C bus, each will have different address by different SA combinations on the PCB. In the check box shown below, when the SA is checked, CPU will use address 0x35 to target the corresponding D820 I^2C device address (with SA pulled high).

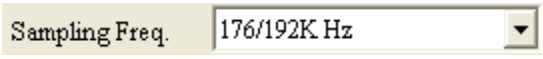


Similarly, if SA is not checked, then D-821Di I^2C device address will be 0x31. The Device Address box will instantly reflect the selected address.

In this development system, the device is communicated with GUI via a USB cable. A command issued by GUI will be translated from USB protocol to I^2C protocol. When the Judge ACK is checked, the GUI tool will check the ACK of the first I^2C command. If the GUI does not receive ACK from D820 after the command is issued, it will show "Device Address Failed" in USB status and a red light. For instance, such a scenario could occur when the USB or I^2C cable is not properly installed, or the slave device cannot be identified.

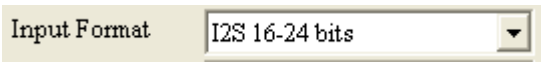
3.9 Sampling rate (FS)





D-821Di can support different input audio sampling rates, ranging from 32K to 192K. The sampling rate is divided in 6 groups: 32k, 44.1/48k, 64k, 88.2/96k, 128k, 176/192k. D820 will handle each sampling rate identically within each group.

3.10 I^2S Input Format



Audio data is sent from system to D820 via I^2S bus. D820 supports I^2S (default), left-alignment, and right-alignment with 16, 18, 20 and 24 bit precision.

3.11 Post Scale Link

This is used in conjunction with 2.3. When "Use CH1 Postscale" is selected, CH2 will use CH1's postscale value specified in 2.3. When "Use Individual Postscale" is selected, each channel will use its own postscale value specified in 2.3.

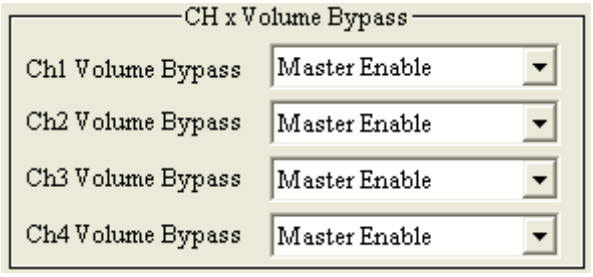
3.12 Left and Right Channel Exchange

When L/R Channel Exchange box is selected, left and right channel (or CH1 and CH2) audio output is exchanged.

3.13 EQ Bypass

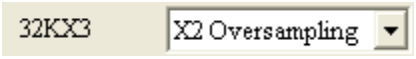
D820 has EQ adjustment described in the EQ control page, which are enabled by this box.

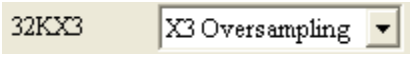
3.14 Master Volume Bypass



As described in 2.1, the net volume control of each channel is the sum of master volume control and channel control. When Master is disabled, the master volume control function is bypassed, and the net volume control is determined by each channel volume control only.

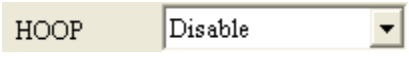
3.15 32KX3

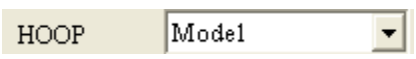


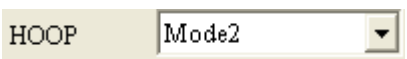


When audio sampling rate is 32k, the default x2 oversampling ratio can be increased to x3 oversampling ratio. Activating this feature, it is possible to have a 96kHz DSP processing when 32kHz used. The PWM carrier frequency of this feature is the same as FS=48K. User needs set 32Kx3 before sending audio data or give a mute command to avoid abnormal sounds.

3.16 HOOP



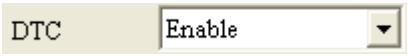




Changing HOOP mode will change PWM frequency. User need set before sending audio data or give a mute command to avoid abnormal sounds

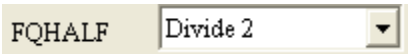
F_S (kHz)	$F_{CARRIER}$ (kHz)/HOPP="0"	HOPP="1"	HOPP="2"	HOPP="3"
32,64,128	1,024	819.2	682.7	Reserved
44.1,88.2,176.4	706	806.4	940.8	Reserved
48,96,192	768	877.7	1024	Reserved

3.17 DTC function



D820 has a built-in Dynamic Temperature Control (DTC) circuits, which is enabled or disabled by this box.

3.18 FQHALF

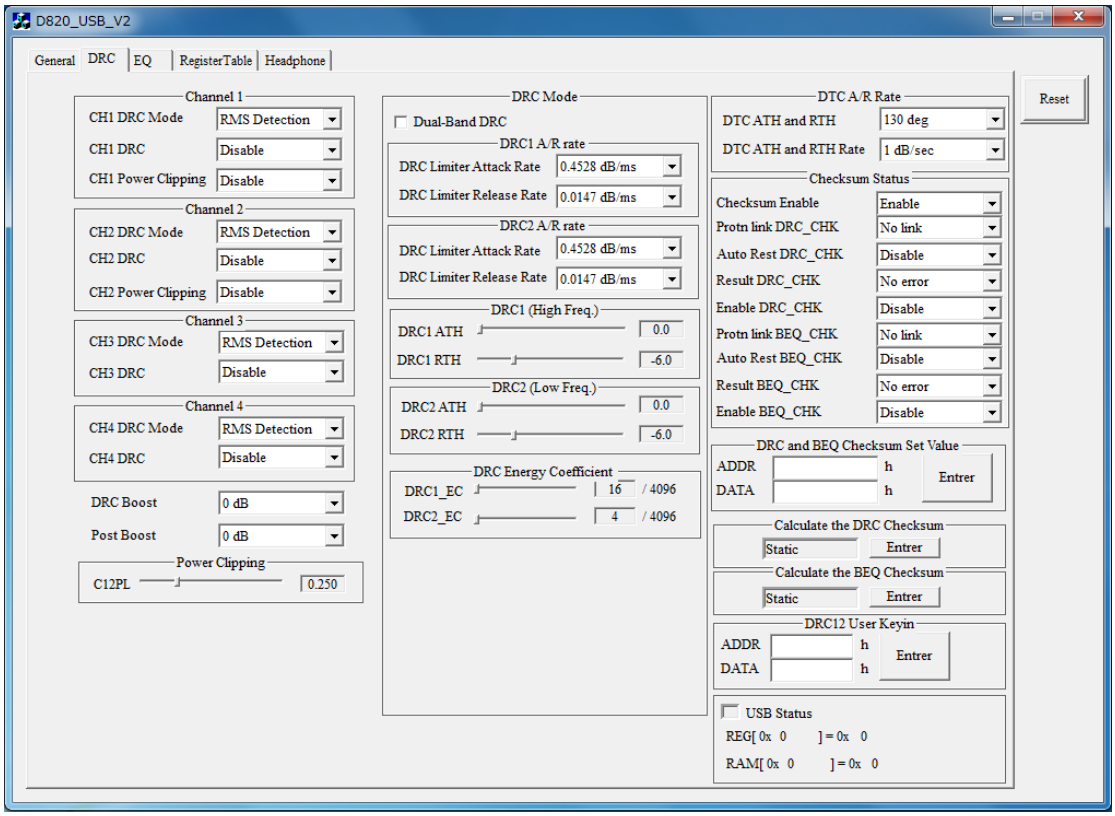


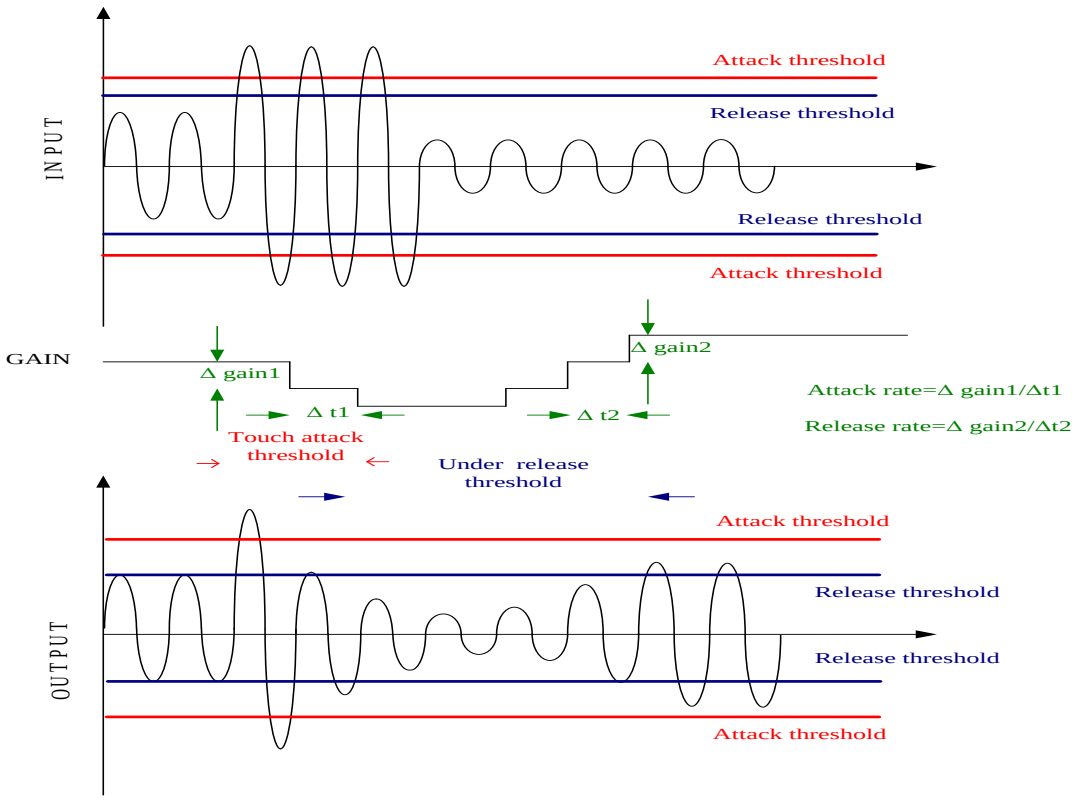
When enable the FAHALF function, the PWM frequency will be divide by 2.

3.19 Amp_Hard_Mute

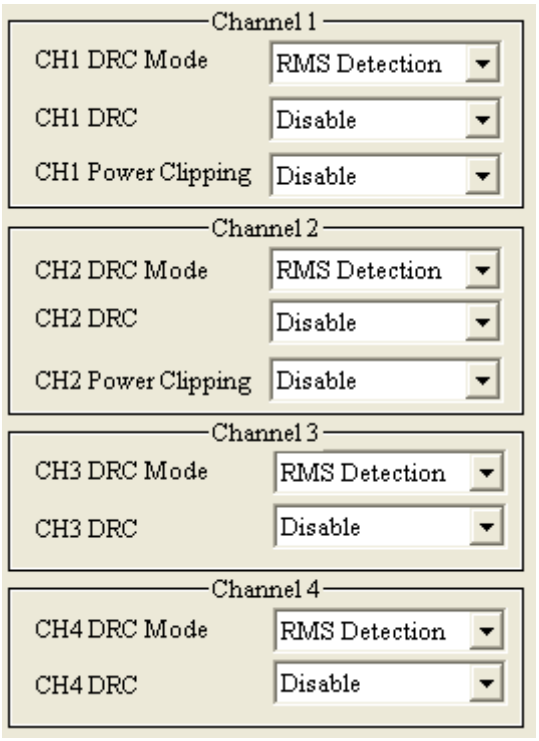
When enable the Amp_Hard_Mute function, the output stage will be turn off.

4. "DRC" Page


D820_USB_V2
General
DRC
EQ
RegisterTable
Headphone
Channel 1
CH1 DRC Mode
RMS Detection
CH1 DRC
Disable
CH1 Power Clipping
Disable
Channel 2
CH2 DRC Mode
RMS Detection
CH2 DRC
Disable
CH2 Power Clipping
Disable
Channel 3
CH3 DRC Mode
RMS Detection
CH3 DRC
Disable
Channel 4
CH4 DRC Mode
RMS Detection
CH4 DRC
Disable
DRC Boost
0 dB
Post Boost
0 dB
Power Clipping
C12PL
0.250
DRC Mode
Dual-Band DRC
DRC1 A/R rate
DRC Limiter Attack Rate
0.4528 dB/ms
DRC Limiter Release Rate
0.0147 dB/ms
DRC2 A/R rate
DRC Limiter Attack Rate
0.4528 dB/ms
DRC Limiter Release Rate
0.0147 dB/ms
DRC1 (High Freq.)
DRC1 ATH
0.0
DRC1 RTH
-6.0
DRC2 (Low Freq.)
DRC2 ATH
0.0
DRC2 RTH
-6.0
DRC Energy Coefficient
DRC1_EC
16
/ 4096
DRC2_EC
4
/ 4096
DTC A/R Rate
DTC ATH and RTH
130 deg
DTC ATH and RTH Rate
1 dB/sec
Checksum Status
Checksum Enable
Enable
Protn link DRC_CHK
No link
Auto Rest DRC_CHK
Disable
Result DRC_CHK
No error
Enable DRC_CHK
Disable
Protn link BEQ_CHK
No link
Auto Rest BEQ_CHK
Disable
Result BEQ_CHK
No error
Enable BEQ_CHK
Disable
DRC and BEQ Checksum Set Value
ADDR
h
DATA
h
Entrer
Calculate the DRC Checksum
Static
Entrer
Calculate the BEQ Checksum
Static
Entrer
DRC12 User Keyin
ADDR
h
DATA
h
Entrer
USB Status
REG[0x 0] = 0x 0
RAM[0x 0] = 0x 0
Reset

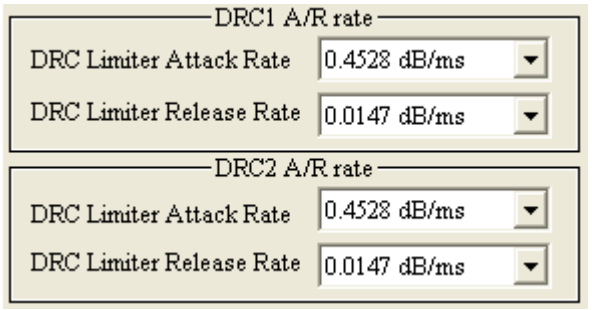

INPUT
Attack threshold
Release threshold
Release threshold
Attack threshold
GAIN
Δ gain1
Δ gain2
Δ t1
Δ t2
Attack rate=Δ gain1/Δt1
Release rate=Δ gain2/Δt2
Touch attack threshold
Under release threshold
OUTPUT
Attack threshold
Release threshold
Release threshold
Attack threshold

4.1 DRC and Power Clipping Bypass



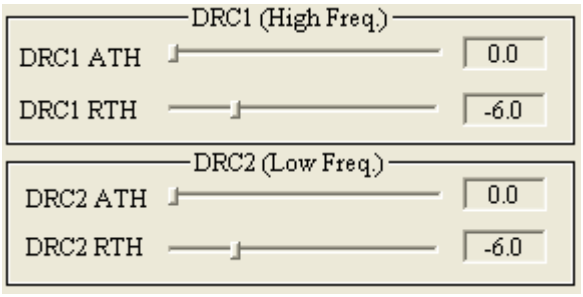
D820 has Dynamic Range Control (DRC) and Power Clipping functions for each channel, which are enabled or disabled by this box.

4.2 DRC Rate



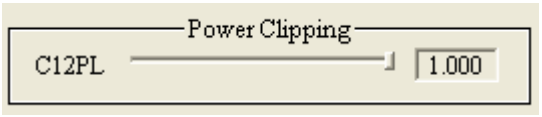
When audio signal reaches DRC Threshold (3.3), the volume is increased or decreased according to the Attack rate or Release rate. The default setting for attack rate is .04528dB/ms, while the default setting for release rate is .0.0147dB/ms.

4.3 DRC threshold



DRC has user_defined attack threshold and release threshold levels, selected by slider. DRC1 is set for CH1 and CH2 and DRC2 is set for CH3.

4.4 Power Clipping

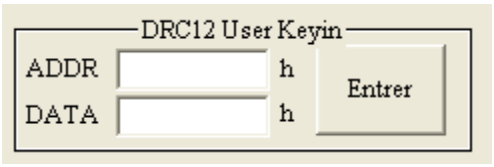


D820 has a power clipping function to prevent speakers from being damaged due to excessive audio power. C12PL box selects power limit value between 0 and 1, which controls CH1 and CH2. The default value is 1.

The power clipping level is defined by 24-bit representation. The following table shows the power clipping level's numerical representation.

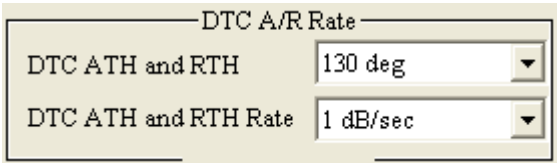
Max amplitude	dB	Linear	Hex
PVDD	0	1	7FFFFF
PVDD*0.707	-3	0.707	5A7EF9
PVDD*0.5	-6	0.5	3FFFFF

4.5 DRC user key in



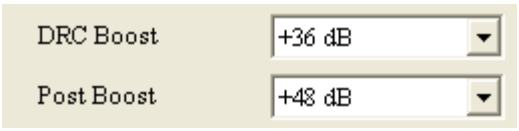
In 3.3, the addresses of DRC1 ATH, RTH, and DRC2 ATH, RTH are 0x81, 82, 83, and 84, respectively. In addition to using the slide bar in 3.3 for entering their values, they can also be entered in this field. For instance, entering 71 into ADDR and 200000 into DATA will correspond to DRC1 ATH = 0.0 described in 3.3. This field is useful for engineering fine tuning purpose.

4.6 DTC threshold and rate



When audio signal reaches DTC Threshold, the volume is increased or decreased according to the Attack rate or Release rate. The default setting for attack and release rate is 1dB/sec.

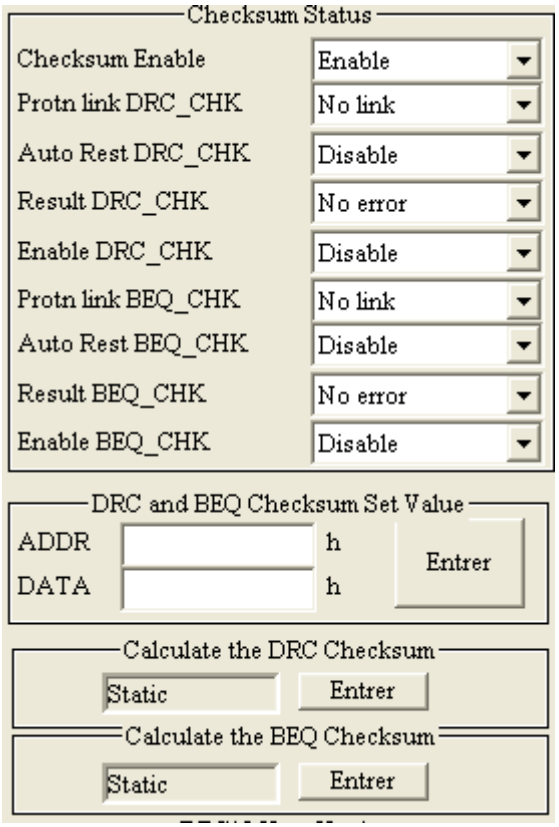
4.7 DRC Boost and Post-scale Boost



When enable DRC Boost function, the audio signal will increase +36dB.

When enable Post Boost function, the audio signal will increase +48dB.

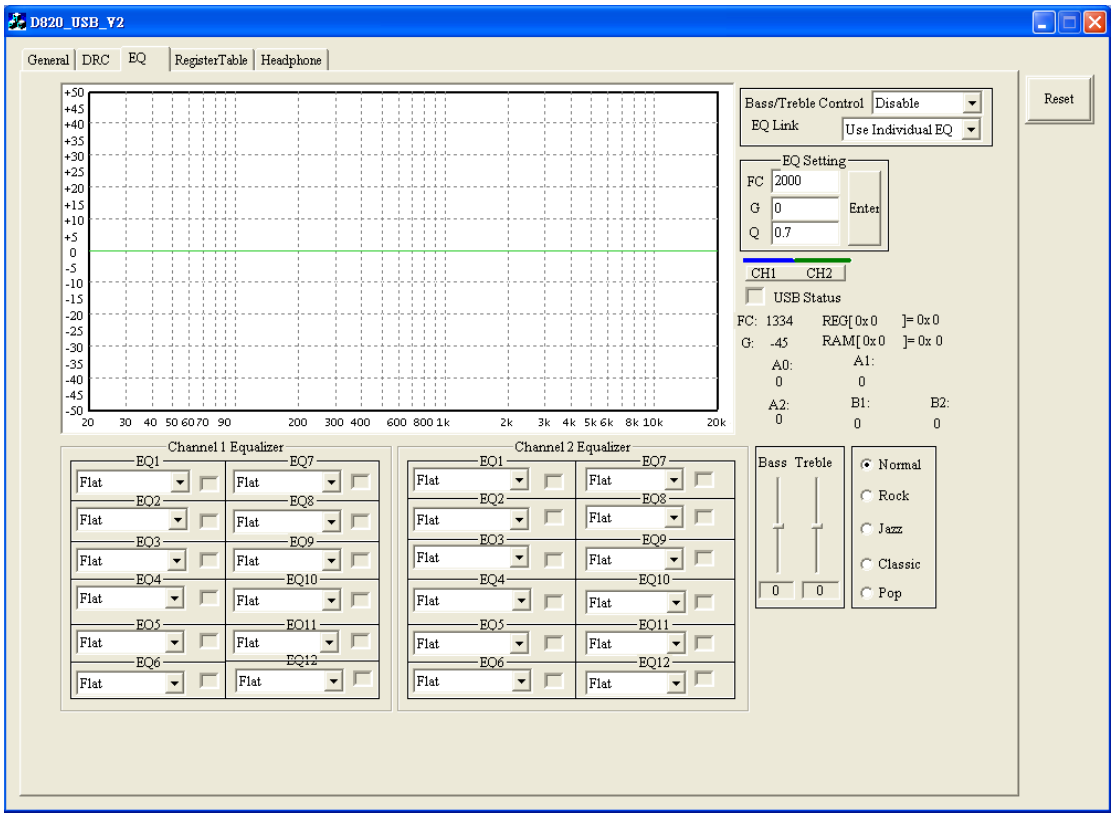
4.8 Checksum Status



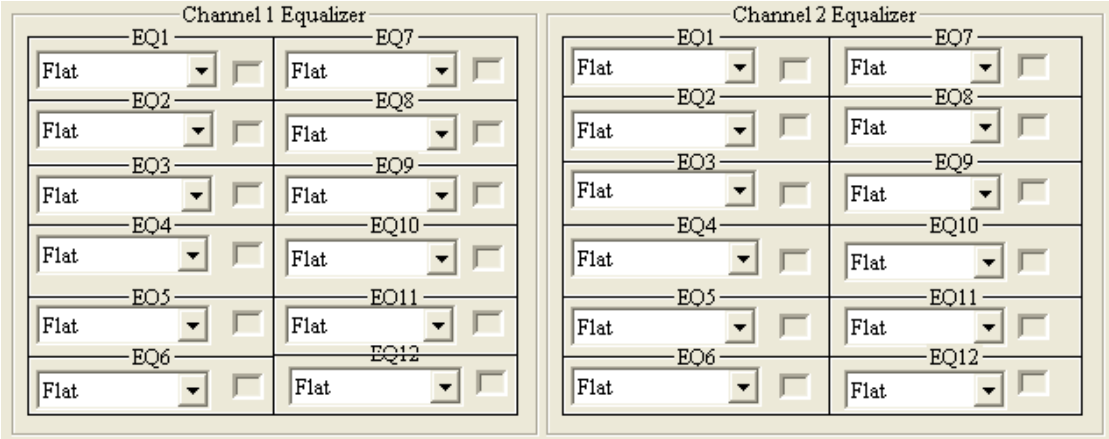
The D820 implements an automatic CRC computation for the BEQ and DRC coefficient RAM. Memory cell contents from address 0x00 to 0x77 will be bit XORed to obtain the BQCHKE checksum, while cells from 0x4B to 0x4D will be XORed to obtain the BEQ_CHK set value.

When CHK_BEQ_EN or CHK_DRC_EN is set to ‘1’, the relative checksum (BQCHKE and DRCCHKE) is continuously compared with BEQ_CHK set value and DRC_CHK set value respectively. If the checksum matches its own reference value, the respective result bits (CHK_DRC_R and CHK_BEQ_R) will be set to ‘0’. The compare bits have no effect if the respective CHK_BEQ_EN or CHK_DRC_EN is not set. In case of checksum errors (i.e. the internally computed didn’t match the reference), an automatic device mute action can be activated. This function is enabled when the CHK_DRC_AR or CHK_BEQ_AR bit is set to ‘1’. The automatic reset bits have no effect if the respective compare bits are not set.

5. “EQ” Page



5.1 Equalizer Filter

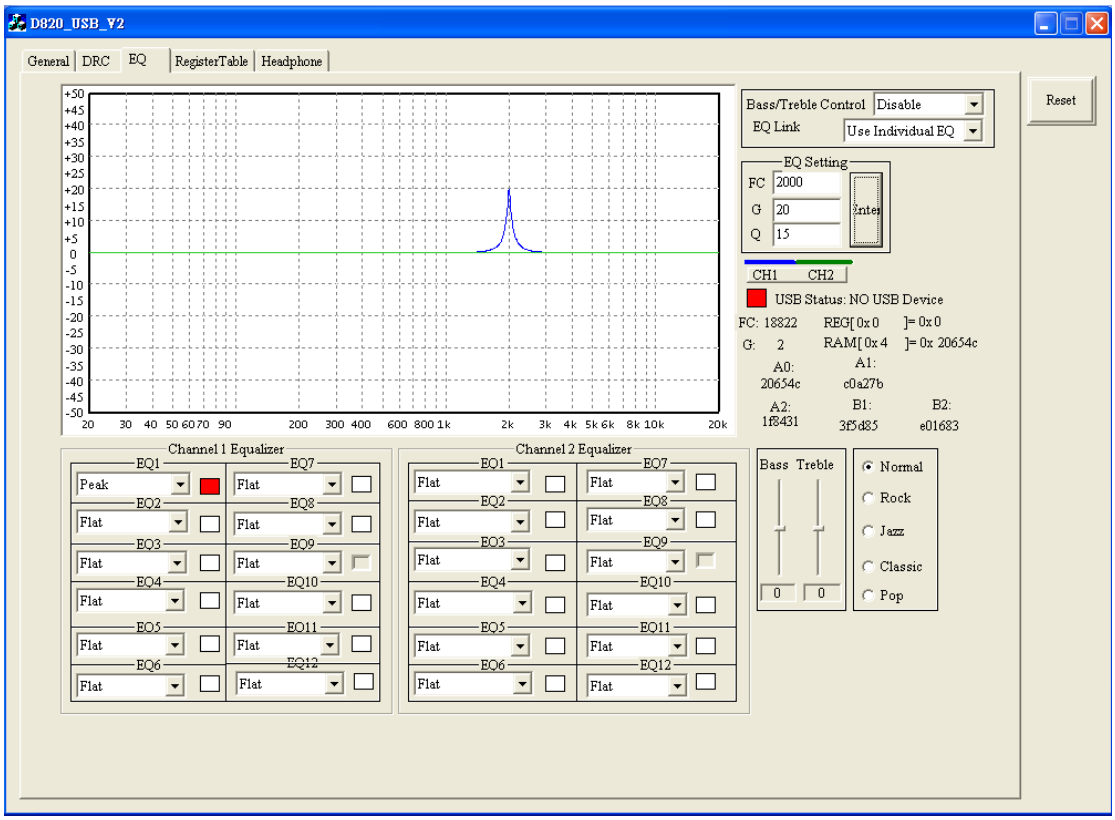


D820 has 12 equalizers for CH1 and CH2

Each equalizer can be adjusted, the defined by FC (Center Frequency), G (Gain), and Q (Qualify Factor). These values can be adjusted either by entering the numerical values in the corresponding box.

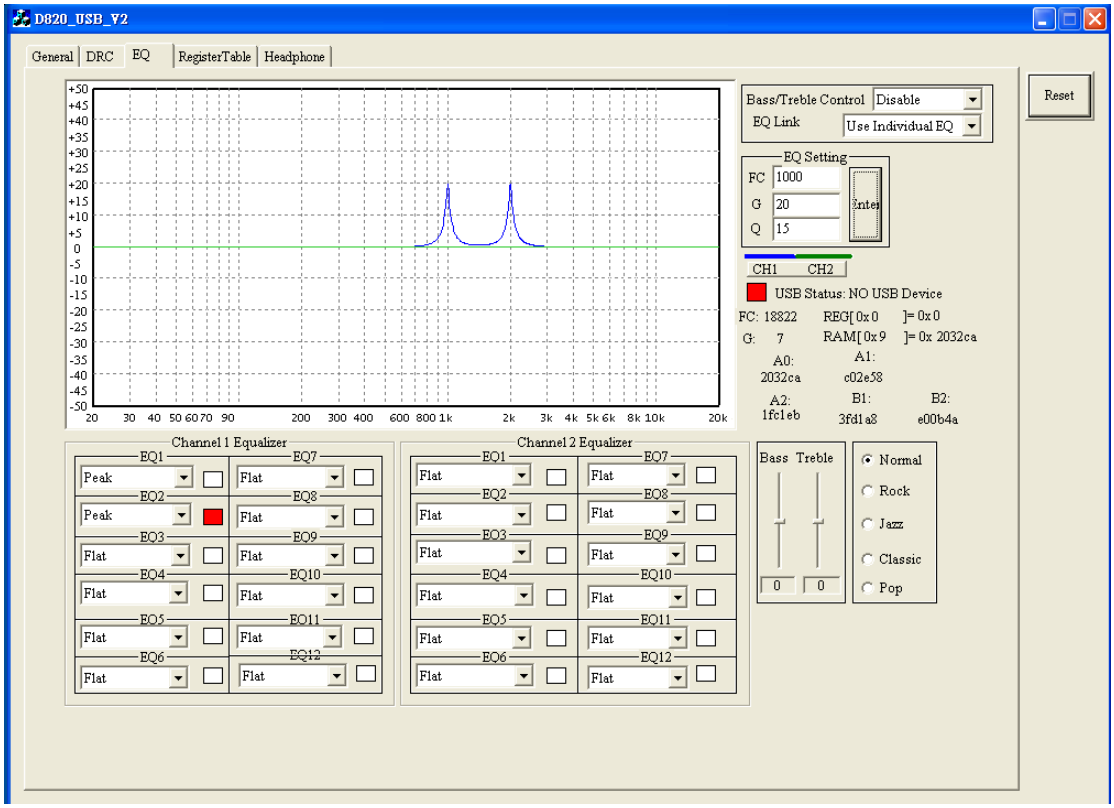
Alternatively, each equalizer can also have the following basic filter selections: Flat, Peak, HPF, LPF, High Shelf, and Low Shelf. Each basic filter can be adjusted by FC, G and Q.

When an equalizer box is adjusted by either method, that filter box is high lighted as red box.

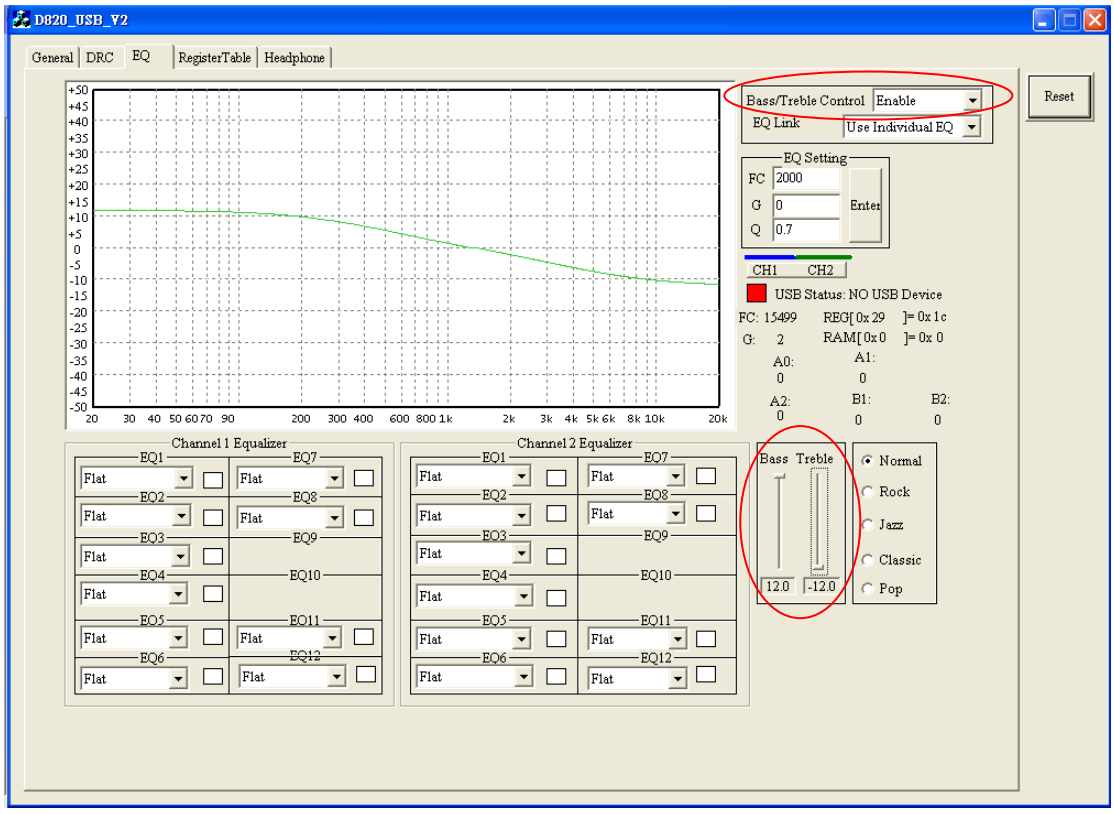


The updated frequency response will be shown in the GUI instantly when any value is adjusted. In the frequency response plot, the X axis is frequency (unit: Hz, in log scale), and the Y axis is gain (unit: dB, in linear scale).

Other than entering the numerical values in the corresponding box for adjustment, a user can also drag the frequency response curve directly to the desired curve position, which will change the values in the corresponding EQ box instantly. Other EQ box can be adjusted similarly when that box is selected,



5.2 Bass and Treble

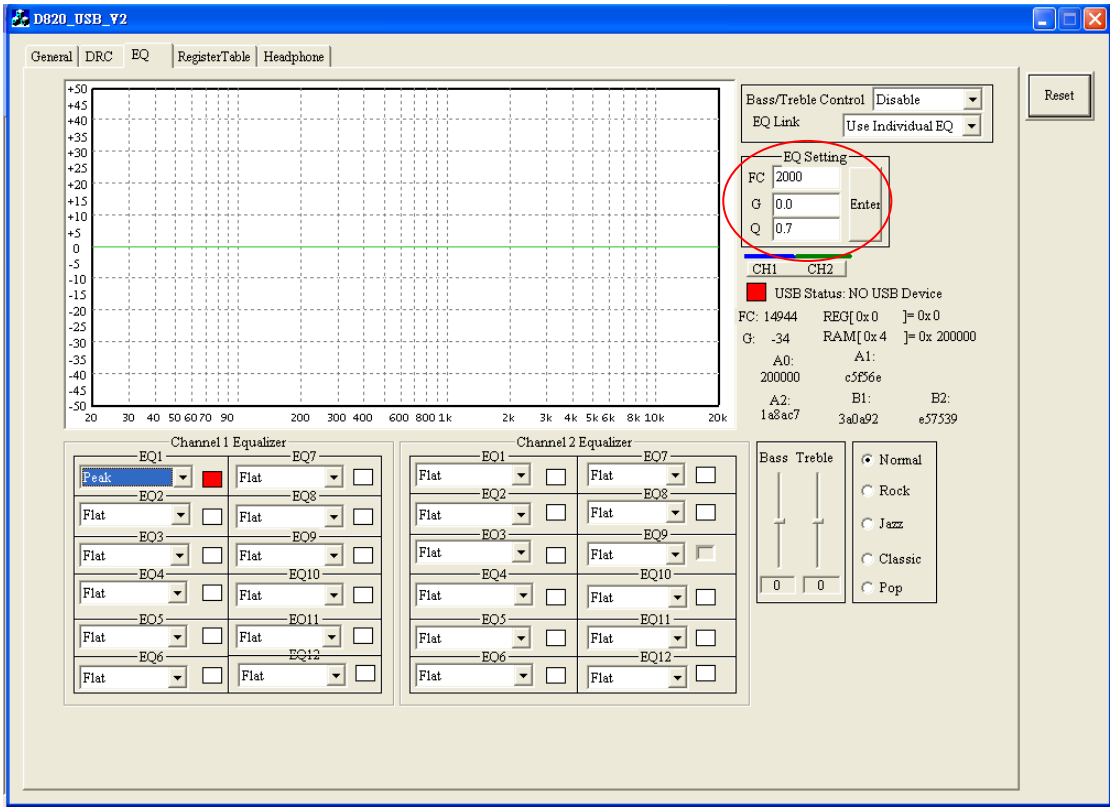


D-821Di has built-in bass and treble controls. When Bass/Treble control is enabled, the last 2 EQ bands of CH1 and CH 2 will become bass and treble control of each channel with preset cutoff frequencies (base = 360Hz, and treble = 7KHz). For instance, EQ9 and EQ10 in the above figure will become bass and treble, and they will be hidden on GUI. However, their frequency response will still be shown on the frequency response curve. The gain of Bass and treble band has 25 levels, from +12dB to -12dB and the default value is 0dB.

5.3 EQ Link

D-821Di, each channel has 12 EQ bands. When use CH1 EQ is selected in the EQ Link combo box, all other channel EQ values will not be used. Instead, the corresponding channel 1 EQ values will be used for other channel EQ values. The default setting is to use individual EQ values.

5.4 EQ setting

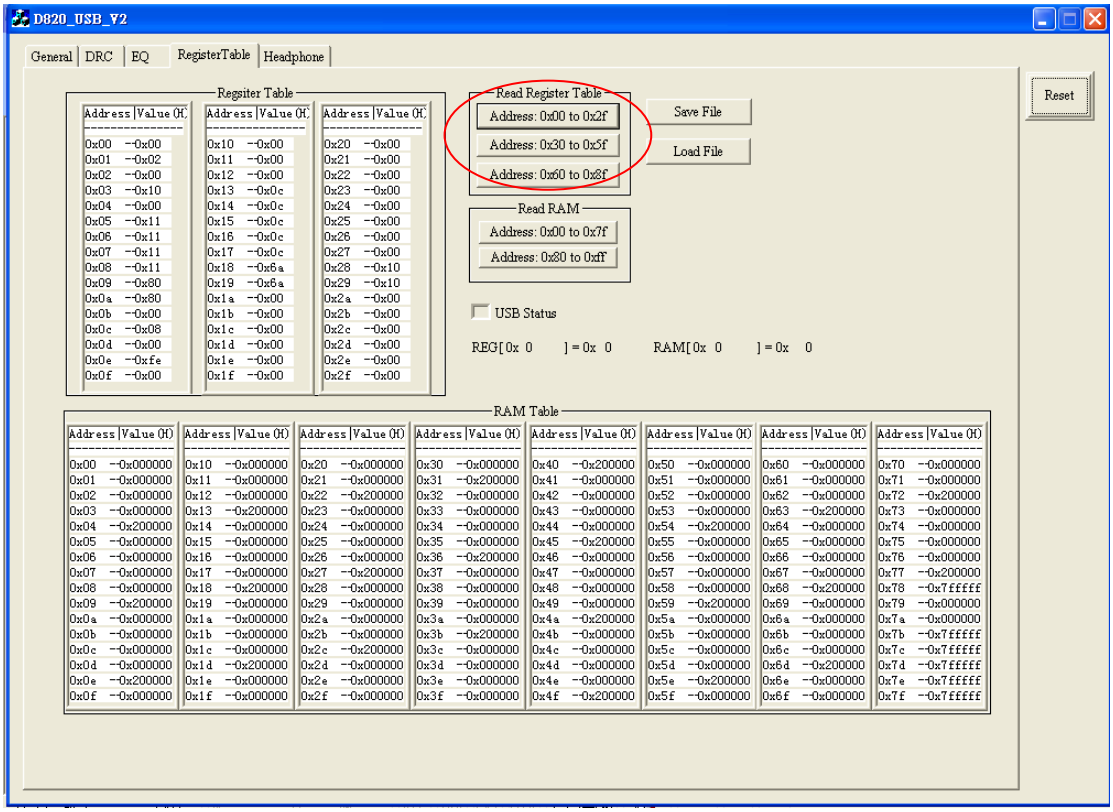


Besides drag the frequency response curve directly to the desired curve position, GUI can also adjust EQ values by keying in values in the selected combo box.

6. *"Register Table" Page*

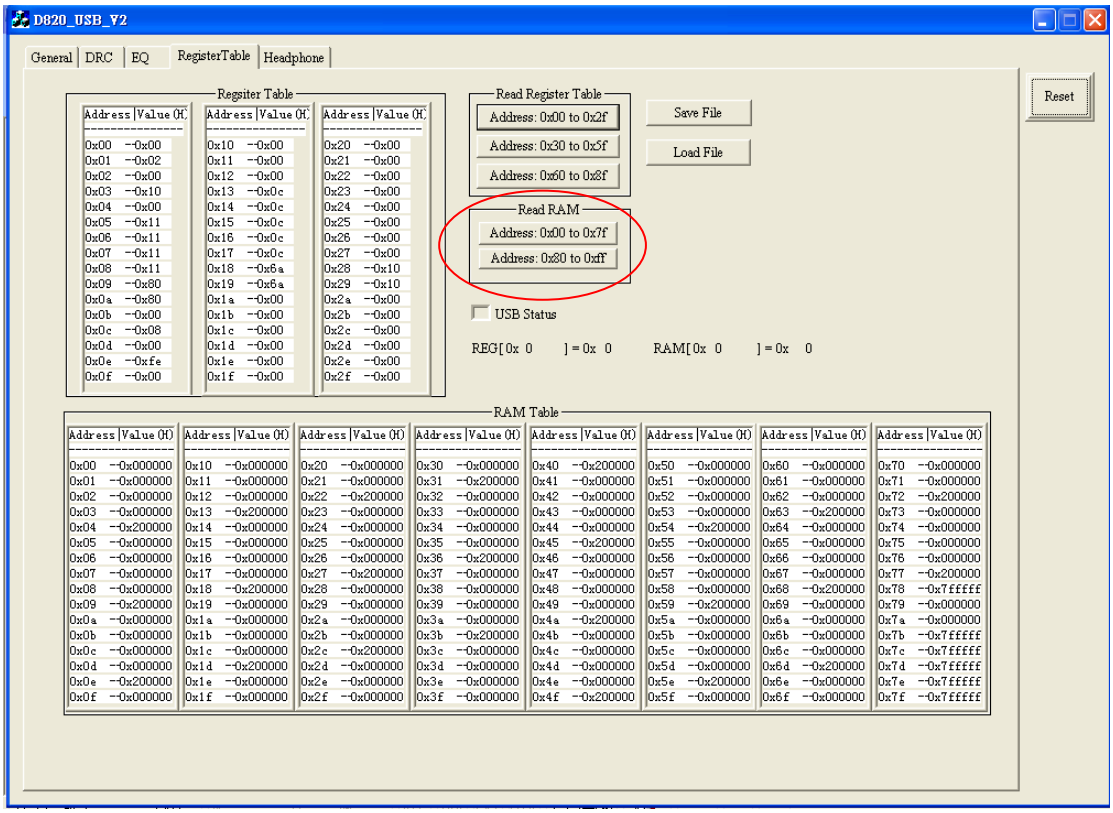
All register values are displayed and individual register bit can be modified in this page. The registers can be stored (SAVE) and retrieved (LOAD) from appropriate buttons in this page.

6.1 Register Table



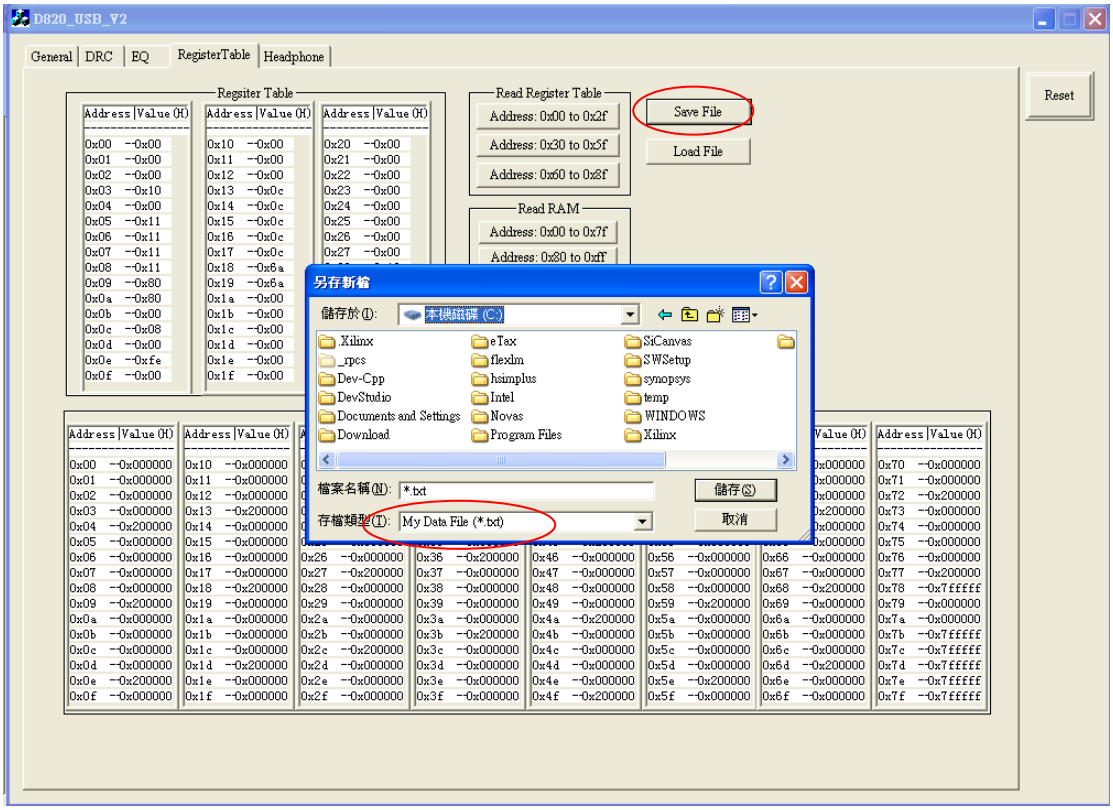
D820 GUI can use the Read Register button to read all register values from D820. And all the registers setting will be shown in the register table.

6.2 RAM Table



D-821Di has 136x24bit of RAM for user programmed items such as filter coefficients. The RAM content can be read out from D820 by the Read RAM button. All RAM content will be shown in the RAM table.

6.3 Save



D-821Di can use SAVE button to store register values, which will generate one file: user_defined.txt. This file has two portions. The first portion shows all register values and RAM contents that are read back from D-821Di. This content will be used by the system developer to build audio driver in the system software. The second portion contains all GUI related information.

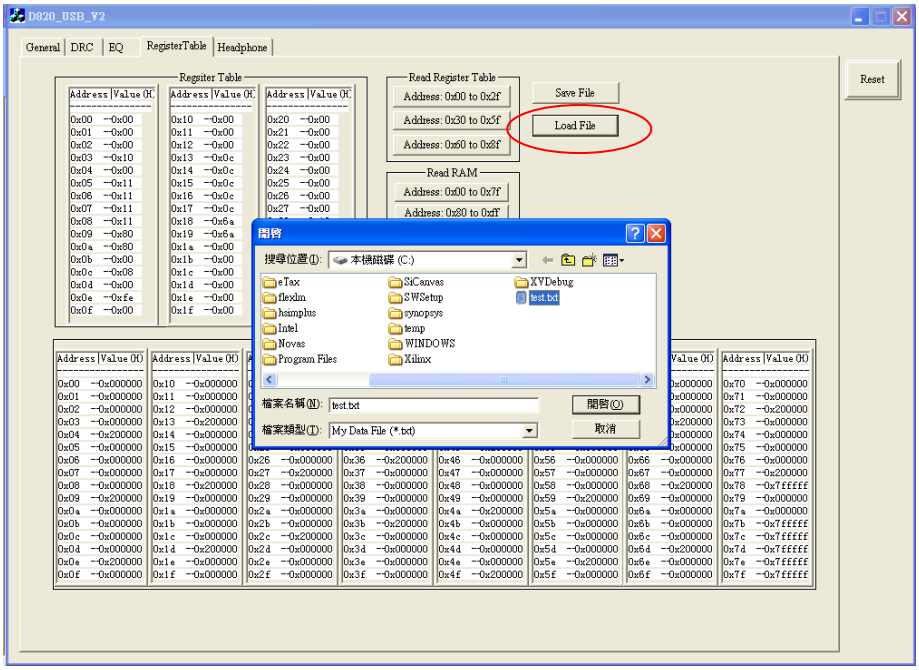
When the LOAD button is pressed, user_defined.txt is used by GUI to generate the previously saved register values and RAM contents.

The user_defined.txt file has the following format (values are in hexadecimal representation).

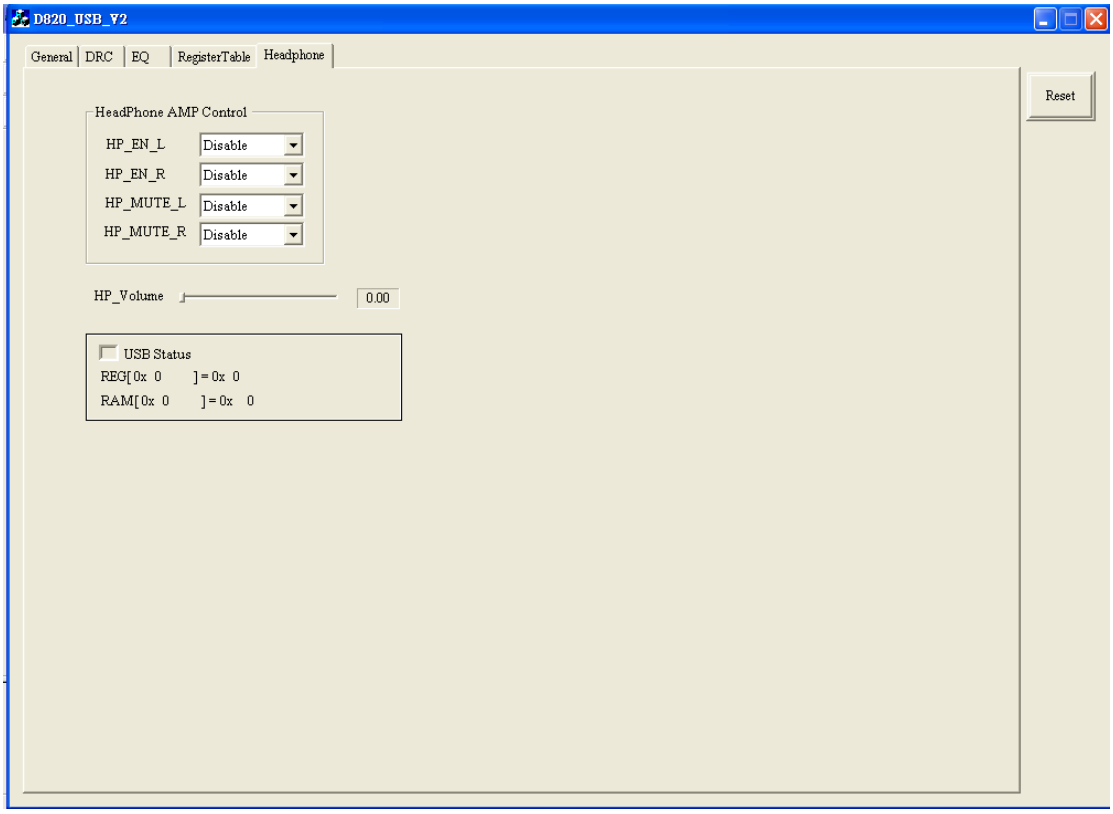
```
1  ############################################################
2  #Product:d820
3  #Date:2014/02/05
4  ############################################################
5
6  ####################Register_Table#####################
7  Reg[00h]=00h ##Device_ID_register_and_Revision_register
8  Reg[01h]=00h ##IF_register
9  Reg[02h]=00h ##MUTE_CM1_CM2_CM3_register
10 Reg[03h]=10h ##LREXC_NG_FADE_EN_DTC_EN_NG_EN_register
11 Reg[04h]=00h ##State_Control
12 Reg[05h]=11h ##Channel_1_configuration_registers
13 Reg[06h]=11h ##Channel_2_configuration_registers
14 Reg[07h]=11h ##Channel_3_configuration_registers
15 Reg[08h]=11h ##Channel_4_configuration_registers
16 Reg[09h]=80h ##HVUV_EN_HV_UVSEL_LV_UVSEL_register
17 Reg[0Ah]=80h ##DTC_TH_DTC_RATE_register
18 Reg[0Bh]=00h ##ERROR_delay_register
19 Reg[0Ch]=08h ##Protection_circuit_register
20 Reg[0Dh]=00h ##Memory_BIST_register
21 Reg[0Eh]=feh ##ERROR_Status_register
22 Reg[0Fh]=00h ##PWM_control_register
23 Reg[10h]=00h ##Test_Mode_register
24 Reg[11h]=00h ##Volume_FT_register
25 Reg[12h]=00h ##C4V_FT_register
26 Reg[13h]=0ch ##MV_register
27 Reg[14h]=0ch ##C1V_register
28 Reg[15h]=0ch ##C2V_register
29 Reg[16h]=0ch ##C3V_register
30 Reg[17h]=0ch ##C4V_register
31 Reg[18h]=6ah ##LA1_and_LR1_register
```

6.4 Load

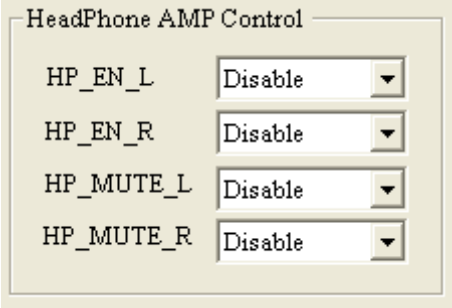
D-821Di can use LOAD button to load user_defined.txt to program the previously saved register and RAM values.



7. "Headphone" Page



7.1 Head Phone AMP Control



When enable HP_EN_L or HP_EN_R function, the LCH or RCH of headphone will enable.

When enable HP_MUTE_L or HP_ MUTE _R function, the LCH or RCH of headphone will be mute.

7.2 Head Phone Volume Control

Head phone volume control ranges from 0dB to +24dB with .25dB increment. The volume for headphone shown in the above box.

PRELIMINARY

March 28, 2014

NOTICE The information provided is preliminary, and subject to change without notice.
Please check for the latest information when using this product in your design.

AGENT

YAMAHA CORPORATION

Address Inquiries to :
Semiconductor Sales & Marketing Department

■Head Office 203, Matsunokijima, Iwata,
Shizuoka, 438-0192, Japan
Tel. +81-539-62-4918 Fax.+81-539-62-5054

■Tokyo Office 2-17-11, Takanawa, Minato-ku,
Tokyo, 108-8586, Japan
Tel. +81-3-5488-5431 Fax.+81-3-5488-5088

■Osaka Office Universal City Wako Bldg.
6-2-82, Shimaya, Konohana-ku,
Osaka, 554-0024, Japan
Tel. +81-6-6465-0325 Fax.+81-6-6465-0391

Printed in Japan