

## YDA184(D-820Di) Evaluation Board

## **Control Software**

## **User Manual**

#### 1. Function Description

D-820Di Control Software is the application which controls the function of D-820Di. Volume control, DRC control, etc. can be operated by accessing the built-in register of D-820Di through USB I/F.

#### 2. Procedure

- (1) Copy "D820 Di\_USB\_V2.2.exe" and "UsbToI2cDll.dll" to the same folder on PC.
- (2) D-820Di evaluation board is connected to PC with an attached USB cable.
- (3) D-820Di evaluation board is power on.
- (4) "D820 Di\_USB\_V2.2.exe" is started. The following GUI is displayed.

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The control is divided into 5 pages: General, DRC, EQ, Register Table, and Headphone. In each page, each field is enclosed by a solid box. Each solid box will be described in this manual, from top to bottom and from left to right order.

Each page has a RESET button on the top right corner. When this button is pressed, registers in all pages will be reset to the default values.

On the General and DRC pages, the register that is adjusted will be instantly reflected in the REG[0x0] = 0x0 field.

The following four GUI selection methods are defined:

Check box: when this box is checked, a specific function is selected.

Slider: when a range of value is to be selected, sliding this bar.



Combo box: for multiple selections.



Edit box: numerical value can be entered here (in HEX format)





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### 3. "General" Page

General DRC EQ RegisterTable Headphone         Master       J 0.0 Mute         CH1       0.0 Mute         CH2       0.0 Mute         CH3       J 0.0 Mute         CH4       J 0.0 Mute         CH1       J 0.0 Mute         CH2       0.0 Mute         CH3       J 0.0 Mute         CH1_MIX1       J 0.0 Mute         CH1_MIX2       J 0.000         CH2       0.000         CH2       0.000         CH2_MIX1       J 0.000         CH2_MIX1       J 1.000         Prescale CH1       J 1.000         Postscale CH1       J 1.000         Postscale CH2       J 1.000	C1 FT       J       0.000       I         C2 FT       J       0.000       I         C3 FT       J       0.000       I         C4 FT       J       0.000       I         HV_UV SEL       4.0 V       I         Noise Gate Level       V       I         Noise Gate Level       V       I         Noise Gate Level       I       I         NG_GAIN       x1/8       I         NG_FADE       Fade       I         IOOP       I-110.0       I         32KX3       X2 Oversampling       I         HOOP       Disable       I         DTC       Disable       I         FOHALF       Default       I	Sampling Freq. 44.1/48K Hz ▼ Input Format 12S 16-24 bits ♥ Post-Scale Link Use Individual Postscale ♥ LR Channel Exchanged NO Exchanged ♥ EQ Bypass Function EQ Enable ♥ Amp_Hard_Mute ♥ CH Volume Bypass Master Enable ♥ Ch1 Volume Bypass Master Enable ♥ Ch2 Volume Bypass Master Enable ♥ Ch3 Volume Bypass Master Enable ♥ Ch4 Volume Bypass Master Enable ♥ Ch4 Volume Bypass Master Enable ♥ Ch4 Volume Bypass Master Enable ♥ IDC Default Setting V Judge ACK Device Address 0x 35 USB Status REG[0x 0] = 0x 0 RAM[0x 0] = 0x 0	Reset

#### 3.1 Volume Adjustment

Volume control consists of 2 parts: master and channel volume control. Each part ranges from -103dB to 6dB with .5dB increment. When Master Volume Bypass is unchecked as described in 2.23, the net volume for each channel shown in the above box (CH1, CH2, CH3 and CH4) is the sum of master and channel volume control. Otherwise, the net volume is determined by each channel volume, e.g., Master volume control is bypassed.

A channel is effectively muted when the net volume is below -103dB, being equivalent to checking the mute box. For the example shown below, Master is set to -103dB, while each channel is set to 0dB, making the volume of each channel set to -103dB.

	Volume
Master	-103.0 🗆 Mute
CH1	
CH2	
CH3	
CH4	[-103.0 🗆 Mute

When each channel's slide bar is moved slightly below 0dB, then each channel is muted, as shown in the following example.





Volume		
Master	Mute 🗆 Mute	
CH1	Mute 🗆 Mute	
CH2	Mute 🗆 Mute	
CH3	Mute 🗆 Mute	
CH4	Mute 🗆 Mute	

#### 3.2 Audio Mixing

Mixing CH1
CH1_MIX1 1.000
CH1_MIX2 0.000
CH2
CH2_MIX1 /
CH2_MIX2 1.000

Audio mixing refers to the function of mixing channel 1 and 2 audio inputs to generate channel 1 and 2 audio outputs. Audio mixing can be additive or subtractive. The mixing range is adjustable by sliding the bar between +.9999 to -1.

In the mixing checking box under CH1, CH1\_MIX1 is the channel 1 mixing proportion to generate channel 1 output, while CH1\_MIX2 is the channel 2 mixing proportion to generate channel 1 output. In the mixing checking box under CH2, CH2\_MIX1 is the channel 1 mixing proportion to generate channel 2 output, while CH2\_MIX2 is the channel 2 mixing proportion to generate channel 2 output.

#### 3.3 Channel Pre and Post Scaling

Prescale CH1	1.000
Prescale CH2	J-1.000
Postscale CH1	
Postscale CH2	J

Prescale is a programmable gain of CH1 and CH2 before any audio processing, while Postscale is a programmable gain of CH1 and CH2 after audio processing. Note the range of scaling is between +.9999 to -1.

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#### 3.4 Volume Fine Tune (VFT)

M FT	l 0.000
C1 FT	L
C2 FT	l 000.0
C3 FT	
C4 FT	

Note that in 2.1, each volume adjustment step is .5dB. When finer volume adjustment is desired, this box specifies the volume fine tune steps with .125dB/step for each channel. 4 selections are provided: 0, -0.125, -0.25, and -0.375dB.

M FT, C1 FT, C2 FT, C3 FT, and C4 FT are applied to Master, CH1, CH2, CH3 and CH4 respectively. For example, if in 2.1, CH1 is selected as -2dB, while in 2.4, CH1 VFT is selected as -0.375dB. Then the net CH1 volume adjustment is -2.375dB.

#### 3.5 High Voltage (HV) Under-Voltage (UV) Protection



D820 has a High Voltage Under-Voltage Protection mechanism. When the high voltage that is applied to the output stage driver drops to a preset value (HV UV detect level), a signal will be generated to trigger the PWM output fade-out function, preventing the annoying pop noise from being generated. Five levels can be selected: 4V (default), 7V, 9V, 12V, and 15V.

#### 3.6 Low Voltage (LV) Under-Voltage (UV) Protection

LV_UV SEL	1.2 V	•
LV_UV SEL	1.4 V	-

D820 has a Low Voltage Under-Voltage Protection mechanism. When the low voltage that is applied to the digital part drops to a preset value (LV UV Detect Level), a signal will be generated to trigger the PWM output fade-out function, preventing the annoying pop noise from being generated. Two levels can be selected: 1.2V (default) or 1.4V,



#### 3.7 Noise gate selection

Noise Gate Level			
Noise Gate Fuction Disable 💌			•
NG_GAIN	x1/8		•
NG_FADE	Fade		•
NGAL -		[-]	110.0
NGRL	-	[.]	100.0

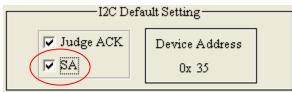
When the Noise Gate function is enabled, D820 will suppress very small input signal further to minimize the output audio noise. In other words, for any audio input signal, when it is less than NGAL, it will be treated as a noise, and its power is further reduced by NG\_GAIN; Otherwise the reduced by NG\_GAIN signal was large than NGRL, the reduced will be release. For instance, in the above selection, when the input signal is less than -110dB, D820 will reduce the signal to 1/8 of the original power. NGAL and NGRL were programmed by user, while NG\_GAIN has 4 values to select: 1/8, 1/4, 1/2, and Mute.

#### 3.8 Communication Interface

In order for the system host CPU to program these on-chip registers to fully utilize D820's flexibility, the industrial standard  $I^2C$  interface is used as the control channel between CPU ( $I^2C$  master) and D820 ( $I^2C$  slave device).

Each  $I^2C$  slave device shall have a unique 7-bit address (device address) for the CPU to identify for communication. In D820, 6 out of 7 device address bits are fixed (0 1 1 0 SA 0 1) inside the chip, while the one bit is defined by one pin, SA, allowing up to two different  $I^2C$  slave devices connected on the same  $I^2C$  bus within the system.

If there are multiple D820 chips on the same  $I^2C$  bus, each will have different address by different SA combinations on the PCB. In the check box shown below, when the SA is checked, CPU will use address 0x35 to target the corresponding D820  $I^2C$  device address (with SA pulled high).





Similarly, if SA is not checked, then D-821Di  $I^2C$  device address will be 0x31. The Device Address box will instantly reflect the selected address.

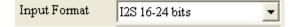
In this development system, the device is communicated with GUI via a USB cable. A command issued by GUI will be translated from USB protocol to  $I^2C$  protocol. When the Judge ACK is checked, the GUI tool will check the ACK of the first  $I^2C$  command. If the GUI does not receive ACK from D820 after the command is issued, it will show "Device Address Failed" in USB status and a red light. For instance, such a scenario could occur when the USB or  $I^2C$  cable is not properly installed, or the slave device cannot be identified.

#### 3.9 Sampling rate (FS)

Sampling Freq.	44.1/48K Hz	•
Sampling Freq.	88.2/96k Hz	-
Sampling Freq.	176/192K Hz	-

D-821Di can support different input audio sampling rates, ranging from 32K to 192K. The sampling rate is divided in 6 groups: 32k, 44.1/48k, 64k, 88.2/96k, 128k, 176/192k. D820 will handle each sampling rate identically within each group.

#### 3.10 I<sup>2</sup>S Input Format



Audio data is sent from system to D820 via  $I^2S$  bus. D820 supports  $I^2S$  (default), left-alignment, and right-alignment with 16, 18, 20 and 24 bit precision.

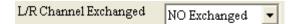
#### 3.11 Post Scale Link

e Individual Postscale	•
	1
	CH1 Postscale

This is used in conjunction with 2.3. When "Use CH1 Postscale" is selected, CH2 will use CH1's postscale value specified in 2.3. When "Use Individual Postscale" is selected, each channel will use its own postscale value specified in 2.3.



#### 3.12 Left and Right Channel Exchange



When L/R Channel Exchange box is selected, left and right channel (or CH1 and CH2) audio output is exchanged.

#### 3.13 EQ Bypass



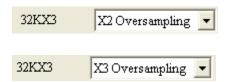
D820 has EQ adjustment described in the EQ control page, which are enabled by this box.

#### 3.14 Master Volume Bypass

CH x Volume Bypass		
Ch1 Volume Bypass	Master Enable 🔹	
Ch2 Volume Bypass	Master Enable 🔹	
Ch3 Volume Bypass	Master Enable 🔹	
Ch4 Volume Bypass	Master Enable 🔹	

As described in 2.1, the net volume control of each channel is the sum of master volume control and channel control. When Master is disabled, the master volume control function is bypassed, and the net volume control is determined by each channel volume control only.

#### 3.15 32KX3



When audio sampling rate is 32k, the default x2 oversampling ratio can be increased to x3 oversampling ratio. Activating this feature, it is possible to have a 96kHz DSP processing when 32kHz used. The PWM carrier frequency of this feature is the same as FS=48K. User needs set 32Kx3 before sending audio data or give a mute command to avoid abnormal sounds.

#### 3.16 HOOP

HOOP	Disable	•
HOOP	Mode1	•
HOOP	Mode2	•



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Changing HOOP mode will change PWM frequency. User need set before sending audio data

F <sub>s</sub> (kHz)	F <sub>CARRIER</sub> (kHz)/HOPP="0"	HOPP="1"	HOPP="2"	HOPP="3"
32,64,128	1,024	819.2	682.7	Reserved
44.1,88.2,176.4	706	806.4	940.8	Reserved
48,96,192	768	877.7	1024	Reserved

or give a mute command to avoid abnormal sounds

#### 3.17 DTC function

DTC Enable -

D820 has a built-in Dynamic Temperature Control (DTC) circuits, which is enabled or disabled by this box.

#### 3.18 FQHALF

FQHALF Divide 2	•
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When enable the FAHALF function, the PWM frequency will be divide by 2.

#### 3.19 Amp\_Hard\_Mute

	Amp_Hard_Mute	Unmute	•
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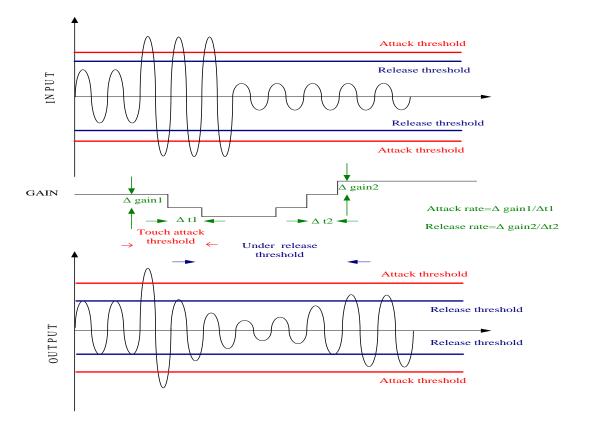
When enable the Amp\_Hard\_Mute function, the output stage will be turn off.



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### 4. "DRC" Page

50 D820_USB_V2			- 🗆 🗙
General DRC EQ RegisterTable Headphone			
Channel 1 CH1 DRC Mode RMS Detection • CH1 DRC Disable • CH1 Power Clipping Disable •	DRC Mode DRC1 A/R rate DRC1 Limiter Attack Rate 0.4528 dB/ms DRC Limiter Release Rate 0.0147 dB/ms DRC Limiter Release Rate 0.0147 dB/ms	DTC A/R Rate DTC ATH and RTH 130 deg TC ATH and RTH Rate DTC ATH and RTH Rate Checksum Status Checksum Enable Enable	<u>.</u>
Channel 2 CH2 DRC Mode RMS Detection • CH2 DRC Disable • CH2 Power Clipping Disable • CH3 DRC Mode RMS Detection • CH3 DRC Disable • CH4 DRC Disable • CH4 DRC Disable • DRC Boost 0 dB • Post Boost 0 dB • Power Clipping 0.250	DRC2 A/R rate DRC Limiter Attack Rate 0.4528 dB/ms DRC Limiter Release Rate 0.0147 dB/ms DRC1 ATH	Protn link DRC_CHK     No link       Auto Rest DRC_CHK     Disable       Result DRC_CHK     Disable       Inable DRC_CHK     Disable       Protn link BEQ_CHK     No link       Auto Rest BEQ_CHK     No link       Auto Rest BEQ_CHK     No link       Protn link BEQ_CHK     No link       Protn link BEQ_CHK     No error       Protn link BEQ_CHK     Disable       OLTA     h       Entrer     DRC12 User Keyin       ADDR     h       Entrer     DISA       Protn link BEQ_CHK     N	
			1





#### 4.1 DRC and Power Clipping Bypass

Channel 1			
CH1 DRC Mode	RMS Detection 💌		
CH1 DRC	Disable 💌		
CH1 Power Clipping	Disable 💌		
Char	unel 2		
CH2 DRC Mode	RMS Detection 💌		
CH2 DRC	Disable 💌		
CH2 Power Clipping	Disable 💌		
Channel 3			
CH3 DRC Mode	RMS Detection 💌		
CH3 DRC	Disable 💌		
Channel 4			
CH4 DRC Mode	RMS Detection 💌		
CH4 DRC	Disable 💌		

D820 has Dynamic Range Control (DRC) and Power Clipping functions for each channel, which are enabled or disabled by this box.

#### 4.2 DRC Rate

DRC1 A/R rate			
DRC Limiter Attack Rate	0.4528 dB/ms 💌		
DRC Limiter Release Rate	0.0147 dB/ms 💌		
DRC2 A/	R rate		
DRC2 A/ DRC Limiter Attack Rate	R rate 0.4528 dB/ms		

When audio signal reaches DRC Threshold (3.3), the volume is increased or decreased according to the Attack rate or Release rate. The default setting for attack rate is .04528dB/ms, while the default setting for release rate is .0.0147dB/ms.



#### 4.3 DRC threshold

DRC1 ATH	— DRC1 (High Freq.) —— J————	0.0
DRC1 RTH		-6.0
DRC2 ATH		0.0
DRC2 RTH		-6.0

DRC has user\_defined attack threshold and release threshold levels, selected by slider. DRC1 is set for CH1 and CH2 and DRC2 is set for CH3.

#### 4.4 Power Clipping

[	Power Clipping
C12PL	

D820 has a power clipping function to prevent speakers from being damaged due to excessive audio power. C12PL box selects power limit value between 0 and 1, which controls CH1 and CH2. The default value is 1.

The power clipping level is defined by 24-bit representation. The following table shows the power clipping level's numerical representation.

Max amplitude	dB	Linear	Hex
PVDD	0	1	7FFFFF
PVDD*0.707	-3	0.707	5A7EF9
PVDD*0.5	-6	0.5	3FFFFF

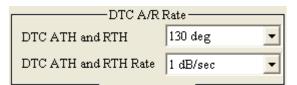
#### 4.5 DRC user key in

DRC12 User Keyin			
ADDR		h	Entrer
DATA		h	Entrel
DATA		n	

In 3.3, the addresses of DRC1 ATH, RTH, and DRC2 ATH, RTH are 0x81, 82, 83, and 84, respectively. In addition to using the slide bar in 3.3 for entering their values, they can also be entered in this field. For instance, entering 71 into ADDR and 200000 into DATA will correspond to DRC1 ATH = 0.0 described in 3.3. This field is useful for engineering fine tuning purpose.



#### 4.6 DTC threshold and rate



When audio signal reaches DTC Threshold, the volume is increased or decreased according to the Attack rate or Release rate. The default setting for attack and release rate is 1dB/sec.

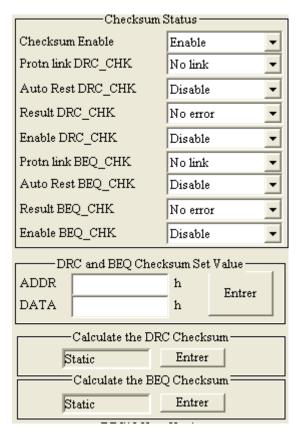
#### 4.7 DRC Boost and Post-scale Boost

DRC Boost	+36 dB	-
Post Boost	+48 dB	-

When enable DRC Boost function, the audio signal will increase +36dB.

When enable Post Boost function, the audio signal will increase +48dB.

#### 4.8 Checksum Status



The D820 implements an automatic CRC computation for the BEQ and DRC coefficient RAM. Memory cell contents from address 0x00 to 0x77 will be bit XORed to obtain the BQCHKE checksum, while cells from 0x4B to 0x4D will be XORed to obtain the BEQ\_CHK set value.

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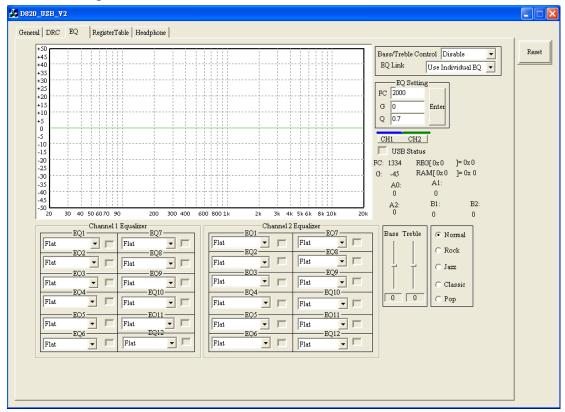
When CHK\_BEQ\_EN or CHK\_DRC\_EN is set to '1', the relative checksum (BQCHKE and DRCCHKE) is continuously compared with BEQ\_CHK set value and DRC\_CHK set value respectively. If the checksum matches its own reference value, the respective result bits (CHK\_DRC\_R and CHK\_BEQ\_R) will be set to '0'. The compare bits have no effect if the respective CHK\_BEQ\_EN or CHK\_DRC\_EN is not set. In case of checksum errors (i.e. the internally computed didn't match the reference), an automatic device mute action can be activated. This function is enabled when the CHK\_DRC\_AR or CHK\_BEQ\_AR bit is set to '1'. The automatic reset bits have no effect if the respective compare bits are not set.

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### 5. "EQ" Page



#### 5.1 Equalizer Filter

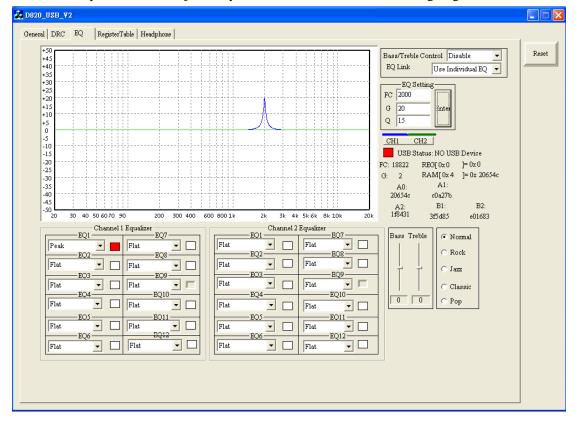
EQ1 — EQ1	alizer EQ7			Equalizer	-EQ7
Flat Flat	t 🔽	Flat		Flat	
Flat Fla		Flat	EO3	F1at	-EQ9
Flat Flat		Flat	- <b>-</b>	Flat	•
Flat 🔽 Fla		Flat	EQ4	Flat	-EQ10
Flat Fla	EQ11 t EQ12	Flat	ЕО5 ЕО6	Flat	-EQ11
EQ6		Flat		Flat	-EQ12

D820 has 12 equalizers for CH1 and CH2

Each equalizer can be adjusted, the defined by FC (Center Frequency), G (Gain), and Q (Qualify Factor). These values can be adjusted either by entering the numerical values in the corresponding box.

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Alternatively, each equalizer can also have the following basic filter selections: Flat, Peak, HPF, LPF, High Shelf, and Low Shelf. Each basic filter can be adjusted by FC, G and Q.



When an equalizer box is adjusted by either method, that filter box is high lighted as red box.

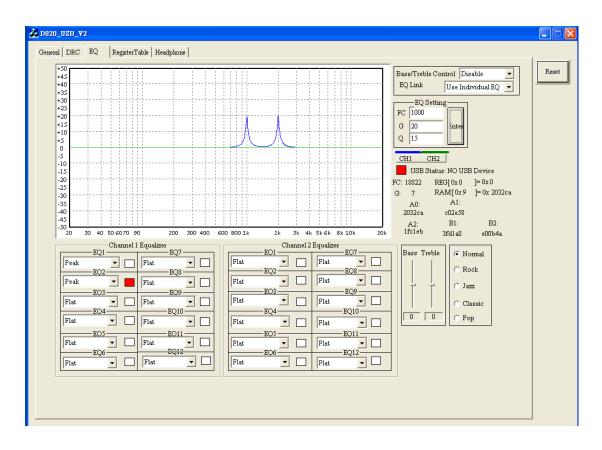
The updated frequency response will be shown in the GUI instantly when any value is adjusted. In the frequency response plot, the X axis is frequency (unit: Hz, in log scale), and the Y axis is gain (unit: dB, in linear scale).

Other than entering the numerical values in the corresponding box for adjustment, a user can also drag the frequency response curve directly to the desired curve position, which will change the values in the corresponding EQ box instantly. Other EQ box can be adjusted similarly when that box is selected,

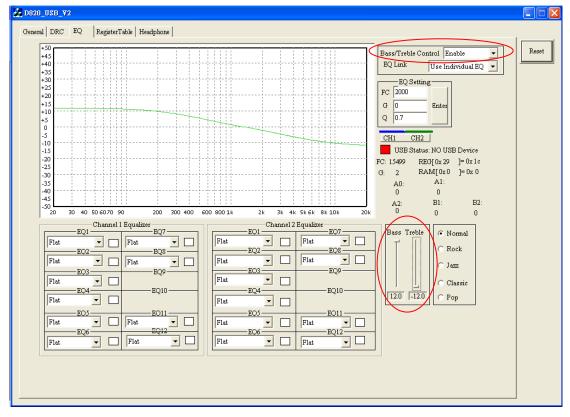
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#### 5.2 Bass and Treble





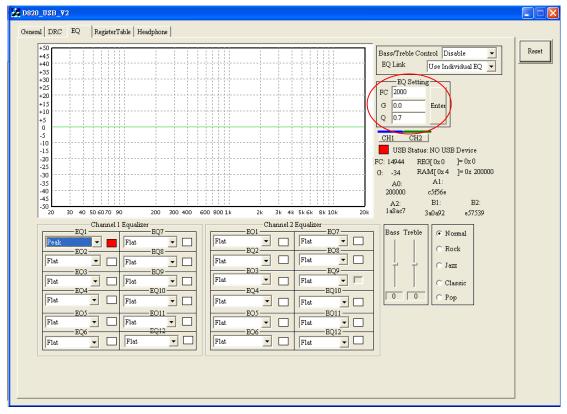
D-821Di has built-in bass and treble controls. When Bass/Treble control is enabled, the last 2 EQ bands of CH1 and CH 2 will become bass and treble control of each channel with preset cutoff frequencies (base = 360Hz, and treble = 7KHz). For instance, EQ9 and EQ10 in the above figure will become bass and treble, and they will be hidden on GUI. However, their frequency response will still be shown on the frequency response curve. The gain of Bass and treble band has 25 levels, from +12dB to -12dB and the default value is 0dB.

#### 5.3 EQ Link

EQ Link	Use Individual 🔻
EQ Link	Use Chi EQ 💌

D-821Di, each channel has 12 EQ bands. When use CH1 EQ is selected in the EQ Link combo box, all other channel EQ values will not be used. Instead, the corresponding channel 1 EQ values will be used for other channel EQ values. The default setting is to use individual EQ values.

#### 5.4 EQ setting



Besides drag the frequency response curve directly to the desired curve position, GUI can also adjust EQ values by keying in values in the selected combo box.

### 6. "Register Table" Page

All register values are displayed and individual register bit can be modified in this page. The registers can be stored (SAVE) and retrieved (LOAD) from appropriate buttons in this page.

#### 6.1 Register Table

Address   Value (H) 	Regsiter Table Address Value 0x10 -0x00 0x11 -0x00 0x12 -0x00		Of Addres	Register Table s: 0x00 to 0x2f s: 0x30 to 0x5f s: 0x60 to 0x8f	Save File Load File			F
0x030x10 0x040x00 0x050x11 0x060x11 0x070x11 0x080x11 0x08 -0x11 0x090x80	0x13 -0x0c 0x14 -0x0c 0x15 -0x0c 0x16 -0x0c 0x17 -0x0c 0x18 -0x6a 0x19 -0x6a	0x23 -0x00 0x24 -0x00 0x25 -0x00 0x26 -0x00 0x27 -0x00 0x27 -0x00 0x28 -0x10 0x29 -0x10	Addres	ead RAM s: 0x00 to 0x7f s: 0x80 to 0xff				
0x080x80 0x0b0x00 0x0c0x08 0x0d0x00 0x0e0xfe 0x0f0x00	0x1s         0x0a           0x1a         -0x00           0x1b         -0x00           0x1c         -0x00           0x1d         -0x00           0x1d         -0x00           0x1d         -0x00           0x1f         -0x00	0x2s -0x10 0x2a -0x00 0x2b -0x00 0x2c -0x00 0x2d -0x00 0x2e -0x00 0x2e -0x00 0x2f -0x00	T USB : REG[0x		RAM[Ox 0	] = 0x 0		
			RAM					
0x000x000000 0	ddress  Value(H) x100x000000 x110x000000		0x30 -0x000000	0x40 -0x200000	0x50 -0x000000	Address Value (H) 0x60 -0x000000 0x61 -0x000000	0x70 -0x000000	
0x020x000000 0 0x030x000000 0	x11 -0x000000 x12 -0x000000 x13 -0x200000 x14 -0x000000	0x220x200000 0x230x000000	0x31 -0x200000 0x32 -0x000000 0x33 -0x000000 0x34 -0x000000	0x41 -0x000000 0x42 -0x000000 0x43 -0x000000 0x44 -0x000000	0x51 -0x000000 0x52 -0x000000 0x53 -0x000000 0x54 -0x200000	0x610x000000 0x620x000000 0x630x200000 0x640x000000	0x710x000000 0x720x200000 0x730x000000 0x740x000000	
0x050x000000 0 0x060x000000 0 0x070x000000 0	x150x000000 x160x000000 x170x000000	0x250x000000 0x260x000000 0x270x200000	0x350x000000 0x360x200000 0x370x000000	0x45 -0x200000 0x46 -0x000000 0x47 -0x000000	0x550x000000 0x560x000000 0x570x000000	0x650x000000 0x660x000000 0x670x000000	0x750x000000 0x760x000000 0x770x200000	
0x09 -0x200000 0 0x0a -0x000000 0	x180x200000 x190x000000 x1a0x000000 x1b0x000000	0x290x000000 0x2a0x000000	0x38 -0x000000 0x39 -0x000000 0x3a -0x000000 0x3b -0x200000	0x480x000000 0x490x000000 0x4a0x200000 0x4b0x000000	0x580x000000 0x590x200000 0x5a0x000000 0x5b0x000000	0x68 -0x200000 0x69 -0x000000 0x6a -0x000000 0x6b -0x000000	0x780x7fffff 0x790x000000 0x7a0x000000 0x7b0x7fffff	
0x0c0x000000 0 0x0d0x000000 0 0x0e0x200000 0	x1c0x000000 x1d0x200000 x1e0x000000	0x2c0x200000 0x2d0x000000 0x2e0x000000	0x3c0x000000 0x3d0x000000 0x3e0x000000	0x4c -0x000000 0x4d -0x000000 0x4e -0x000000	0x5c0x000000 0x5d0x000000 0x5e0x200000	0x6c0x000000 0x6d0x200000 0x6e0x000000	0x7c0x7fffff 0x7d0x7fffff 0x7e0x7fffff	
0x0f -0x000000 0	x1f -0x000000	0x2f -0x000000	0x3f -0x000000	0x4f -0x200000	0x5f -0x000000	0x6f -0x000000	0x7f -0x7fffff	

D820 GUI can use the Read Register button to read all register values from D820. And all the registers setting will be shown in the register table.



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#### 6.2 RAM Table

0x00         0x02         0x00         0x22         0x00         0x22         0x00         0x23         0x00         0x23         0x00         0x24         0x00         0x25         0x00         0x26         0x01         0x01         Address:         0x00         0x01         Address:         0x00         0x01         Address:         0x01         Address:         0x01         Address:         0x01         Address:         0x01         Address:         0x01         Address:         0x10         Address:<	I			_1		Register Table	_					R
0x11       -0x00       0x12       -0x00       0x22       -0x00         0x02       -0x00       0x12       -0x00       0x22       -0x00         0x05       -0x11       0x15       -0x00       0x24       -0x00         0x05       -0x11       0x15       -0x00       0x24       -0x00         0x05       -0x11       0x15       -0x00       0x24       -0x00         0x06       -0x11       0x15       -0x00       0x28       -0x00         0x07       -0x11       0x17       -0x00       0x28       -0x00         0x08       -0x11       0x18       -0x00       0x28       -0x00         0x08       -0x10       0x14       -0x00       0x28       -0x00         0x08       -0x10       0x14       -0x00       0x24       -0x00         0x08       -0x10       0x14       -0x00       0x24       -0x00         0x08       -0x10       0x14       -0x00       0x24       -0x00         0x24       -0x00       0x24       -0x00       0x24       -0x00         0x04       -0x00000       0x14       -0x00000       0x24       -0x00000         0x14 <t< td=""><td>Address Value (H)</td><td>Address Value</td><td>(H) Address Value</td><td>0H)</td><td>Addres</td><td>ss: 0x00 to 0x2f</td><td></td><td>ave File</td><td></td><td></td><td></td><td></td></t<>	Address Value (H)	Address Value	(H) Address Value	0H)	Addres	ss: 0x00 to 0x2f		ave File				
Dedd         -Ox00         Dedd         -Ox00 <t< td=""><td>0x01 -0x02</td><td>0x11 -0x00</td><td>0x21 -0x00</td><td></td><td></td><td></td><td>L</td><td>.oad File</td><td></td><td></td><td></td><td></td></t<>	0x01 -0x02	0x11 -0x00	0x21 -0x00				L	.oad File				
0x05       -0x11       0x15       -0x02       0x25       -0x00         0x06       -0x11       0x15       -0x02       0x25       -0x00         0x07       -0x11       0x17       -0x02       0x28       -0x10         0x08       -0x11       0x19       -0x6a       0x29       -0x10         0x08       -0x00       0x14       -0x00       0x28       -0x00         0x04       -0x00       0x14       -0x00       0x22       -0x00         0x14       -0x00000       0x14       -0x00000       0x30       -0x00000       0x30       -0x00000       0x10       -0x00000       0x10       -0x000000       0x30       -0x000000       0x51       -0x000000       0x61       -0x000000       0x71       -0x000000       0x71       -0x000000       0x71       -0x000000       0x71       -0x000000       0x71												
0x06       -0x11       0x16       -0x0       0x28       -0x10         0x07       -0x11       0x18       -0x60       0x28       -0x10         0x08       -0x00       0x18       -0x60       0x28       -0x10         0x08       -0x00       0x18       -0x00       0x28       -0x10         0x08       -0x00       0x14       -0x00       0x28       -0x10         0x04       -0x00       0x14       -0x00       0x28       -0x00         0x16       -0x00       0x28       -0x00       0x28       -0x00         0x16       -0x00       0x14       -0x00       0x24       -0x00000       0x44       -0x00000       0x41       -0x00000       0x41       -0x00000       0x41       -0x00000       0x41       -0x00000       0x41       -0x00000       0x42       -0x00000       0x44					F	lead RAM ———						
Dectr         -Out1         Out1         -Out0         Dock         -Out0					Addre:	ss: 0x00 to 0x7f 📗	<u>۱</u>					
Ducos         -Oxt0         Dicks         -Oxt0 <th< td=""><td></td><td></td><td></td><td></td><td>é ddre</td><td>ee: 0x80 to 0xff</td><td>)</td><td></td><td></td><td></td><td></td><td></td></th<>					é ddre	ee: 0x80 to 0xff	)					
0x0a         -0x80         0x1a         -0x00         0x2b         -0x00000         0x2b         -0x000000         0x2b						55. 0.00 10 0.11	·					
Docb         -Outo0         Doch         -Outo0         Dock												
0x0c         -0x08         0x1c         -0x00         0x2d         -0x00000         0xdd         -0x00000         0xdd         -0x00000         0xdd         -0x000000         0xdd         -0x00000						Statue						
Decle         -Oxfe         Decle         Decle <th< td=""><td></td><td></td><td></td><td></td><td>, 000</td><td>brarab</td><td></td><td></td><td></td><td></td><td></td><td></td></th<>					, 000	brarab						
Date         -0x16         Date         -0x00         Dx2f         -0x00000         Dx2f         -0x00000         Dx2f         -0x000000         Dx3f         -0x000000					REG[0x	0 1=0x 0	RAN	4f0x 0	1 = 0x 0			
RAM Table           Address [Value 00]         Addres [Value 00]         Addres [Value 00] <th< td=""><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></th<>												
Address [Value 00]         Address	0x0f -0x00	0x1f0x00	0x2f -0x00									
Address [Value 00]         Address					DAM	Tabla						
							1	Inc. a. 642		1		
0x01         -0x000000         0x11         -0x000000         0x12         -0x000000         0x12         -0x000000         0x12         -0x000000         0x12         -0x000000         0x13         -0x000000         0x13         -0x000000         0x13         -0x000000         0x13         -0x000000         0x13         -0x000000         0x14         -0x000000         0x14         -0x000000         0x14         -0x000000         0x14         -0x000000         0x15         -0x000000         0x14         -0x000000         0x15         -0x000000         0x14         -0x000000         0x15         -0x000000         0x14         -0x000000         0x16         -0x000000         0x16         -0x000000         0x14         -0x000000         0x14         -0x000000         0x16	Address   Value (H) Ad	idress  Value (H)	Address  Value (H)	Addre:	ss Value (H)	Address  Value (H)	Addre	ss   Value (H)	Address   Value (R)	Address	Value (H)	
0x01         -0x000000         0x11         -0x000000         0x12         -0x000000         0x12         -0x000000         0x12         -0x000000         0x12         -0x000000         0x13         -0x000000         0x13         -0x000000         0x13         -0x000000         0x13         -0x000000         0x13         -0x000000         0x14         -0x000000         0x14         -0x000000         0x14         -0x000000         0x14         -0x000000         0x15         -0x000000         0x14         -0x000000         0x15         -0x000000         0x14         -0x000000         0x15         -0x000000         0x14         -0x000000         0x16         -0x000000         0x16         -0x000000         0x14         -0x000000         0x14         -0x000000         0x16	0x000x000000 0x	100x000000	0x200x000000	0x30	0x000000	0x400x200000	0x50	0x000000	0x600x000000	0x70	0x000000	
0x03         -0x000000         0x13         -0x000000         0x14         -0x000000         0x14         -0x000000         0x14         -0x000000         0x14         -0x000000         0x15         -0x000000         0x15         -0x000000         0x15         -0x000000         0x15         -0x000000         0x15         -0x000000         0x15         -0x000000         0x16         -0x000000         0x16         -0x000000         0x16         -0x000000         0x17         -0x000000         0x16         -0x000000         0x16         -0x000000         0x16         -0x000000         0x16         -0x000000         0x17         -0x000000         0x17         -0x000000         0x17         -0x000000         0x17         -0x000000         0x16         -0x000000         0x16         -0x000000         0x18         -0x000000         0x18         -0x000000         0x14         -0x000000         0x14         -0x000000         0x24         -0x000000         0x24         -0x000000         0x24         -0x000000         0x26         -0x000000         0x16         -0x000000         0x16	0x01 -0x000000 0x	11 -0x000000	0x21 -0x000000	0x31	0x200000	0x410x000000		-0x000000	0x610x000000	0x71	0x000000	
0x14         -0x20000         0x14         -0x00000         0x14         -0x00000         0x14         -0x00000         0x44         -0x00000         0x44         -0x00000         0x45         -0x00000         0x47         -0x00000         0x47         -0x00000         0x46         -0x00000         0x45         -0x00000         0x46         -0x00000         0x45         -0x00000         0x46         -0x00000         0x47         -0x000000         0x46 </td <td></td>												
bnds         -0x000000         bnls         -0x17         bnls         -0x000000 <td></td>												
0x06         -0x00000         0x16         -0x000000         0x17         -0x000000         0x18         -0x000000         0x16         -0x000000         0x17         -0x000000         0x17         -0x000000           0x18         -0x000000         0x18         -0x000000         0x28         -0x000000         0x14         -0x000000         0x56         -0x000000         0x67         -0x000000         0x78         -0x000000         0x68         -0x000000         0x78         -0x000000         0x67         -0x000000												
0x08         -0x000000         0x18         -0x200000         0x18         -0x000000         0x18         -0x000000         0x18         -0x000000         0x18         -0x000000         0x18         -0x000000         0x18         -0x000000         0x78												
0x03         -0x00000         0x19         -0x000000         0x29         -0x000000         0x39         -0x000000         0x49         -0x000000         0x47         -0x000000         0x47         -0x000000         0x49         -0x000000         0x49         -0x000000         0x49         -0x000000         0x49         -0x000000         0x47         -0x000000         0x49         -0x000000         0x40         -0x74         -0x000000         0x40         -0x000000         0x46         -0x000000         0x40         -0x000000         0x40         -0x000000												
0x0a         -0x000000         0x1a         -0x000000         0x7a         -0x000000         0x7b         -0x1fffff           0x0d         -0x000000         0x1d         -0x000000         0x3b         -0x000000         0x5b         -0x000000         0x7b         -0x07fffff         0x7b         -0x1fffff         0x3c         -0x000000         0x4c         -0x000000         0x5c         -0x000000         0x7b         -0x7ffffff         0x6c         -0x000000         0x1d         -0x000000         0x1d         -0x000000         0x1d         -0x000000         0x1d         -0x000000         0x1d         -0x000000         0x6c         -0x000000         0x6c         -0x000000         0x7c         -0x7ffffff         0x6c         -0x000000         0x6c         -0x0fffffff         0x6c         0x6c												
0x0b         -0x000000         0x1b         -0x000000         0x2b         -0x000000         0x3b         -0x000000         0x4b         -0x000000         0x4b         -0x000000         0x4b         -0x000000         0x4b         -0x000000         0x4b         -0x000000         0x7b         -0x7fffff           0x04         -0x000000         0x1a         -0x000000         0x1a         -0x000000         0x7b         -0x7fffff         0x7b         -0x7ffffff           0x04         -0x000000         0x1a         -0x000000         0x3d         -0x000000         0x4d         -0x000000         0x7d         -0x7ffffff         0x7d         -0x7ffffff           0x04         -0x000000         0x1a         -0x000000         0x3d         -0x000000         0x4d         -0x000000         0x6d         -0x000000         0x7d         -0x7ffffff												
0x0e - 0x000000 0x1e -0x000000 0x2e -0x200000 0x3e -0x00000 0x4e -0x000000 0x5e -0x000000 0x6e -0x000000 0x7e -0x7fffff 0x04 -0x000000 0x1e -0x200000 0x3e -0x00000 0x34 -0x000000 0x4e -0x000000 0x5e -0x00000 0x7e -0x7fffff												
0x0e0x200000 0x1e0x000000 0x2e0x000000 0x3e0x000000 0x4e0x000000 0x5e0x200000 0x6e0x000000 0x7e0x7fffff	0x0c0x000000 0x	1c -0x000000	0x2c -0x200000	0x3c	0x000000	0x4c0x000000	0x5c	0x000000	0x6c0x000000	0x7c	0x7fffff	
	10x01 0x000000 103	.11 02000000	0x21 0x000000	JOXOT	0x000000	0x200000	Joxor	0x000000	0x01 0x000000	lloxit	OXTILLI	

D-821Di has 136x24bit of RAM for user programmed items such as filter coefficients. The RAM content can be read out from D820 by the Read RAM button. All RAM content will be shown in the RAM table.



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#### 6.3 Save

	—Regsiter Table —				Register	r Table —	-						Re
Address Value (H)	Address Value (H)	Address Value	00	Addres	ss: 0x00	to 0x2f	5	ave File					
0x000x00	0x10 -0x00	0x20 -0x00		Addre	ss: 0x30	to 0x5f	<u> </u>						
0x01 -0x00	0x110x00	0x210x00						oad File					
0x02 -0x00 0x03 -0x10	0x120x00 0x130x0c	0x220x00 0x230x00		Addre:	ss: 0x60	to 0x8f							
0x04 -0x00	0x13 -0x0c	0x24 -0x00			lead RA	M							
0x05 -0x11	0x15 -0x0c	0x250x00											
0x06 -0x11	0x160x0c	0x260x00				to 0x7f							
0x07 -0x11 0x08 -0x11	0x170x0c 0x180x6a	0x27 -0x00		Addre	ss: 0x80	to Oxff							
0x08 -0x11 0x09 -0x80		另存新檔							<b>?</b> ×				
0x0a0x80	0x1a0x00									1			
0x0b0x00	0x1b0x00	儲存於①: <	▶ 本機	磁碟 (C:)		-	¢	🗈 💣 🎟 •					
0x0c0x08 0x0d0x00	0x1c0x00 0x1d0x00	Cilinx Cilinx		🚞 e Tax		6	SiCanv	'8.S	6				
0x0e -Oxfe	0x1e0x00	rpcs		🛅 flexim			SWSet		_				
0x0f -0x00	0x1f -0x00	Dev-Cpp		🛅 hsimpl			synops						
	<u> </u>	🛅 DevStudio		🛅 Intel		_	temp						
		🛅 Documents an	d Setting	ps 🛅 Novas			WIND	OWS					
Address Value (H) Ad	dress Value (H) 🕴	🚞 Download		🛅 Progra	m Files	<u> </u>	Xilinx			Value (H)	Addre	ss Value (H)	
0x00 -0x000000 0x	100x000000 0	<							>	0x000000	0.70	0x000000	
0x00 -0x000000 0x		<u>e</u>					_	-	_	0x0000000	0x70	0x000000	
0x020x000000 0x	120x000000 0	檔案名稱(N): *	.bd					儲存(S)		0x00000x0	0x72	0x200000	
0x03 -0x000000 0x		存檔類型(I): 🕨	(v Data I	Zilo (# tod)			-	取消	1	0x200000	0x73	0x000000	
0x04 -0x200000 0x 0x05 -0x000000 0x	14 -0x000000 0 15 -0x000000 0		iy Dala i	une (Clark)	$\mathcal{I}$		<u> </u>			Dx000000	0x74 0x75	0x000000 0x000000	
0x05 -0x000000 0x		c26 −0x000000	0x36	0x200000	0x46	0x000000	0x56	-0x000000	0x66	-0x0000000	0x15	0x000000	
0x070x000000 0x	170x000000 0x	27 -0x200000	0x37	0x000000	0x47	0x000000	0x57	0x000000	0x67 ·	-0x000000	0x77	0x200000	
0x080x000000 0x		28 -0x000000		-0x000000		0x000000	0x58	0x000000		-0x200000	0x78	-0x7fffff	
		c290x000000 c2a0x000000		0x000000 0x000000	Ox49 Ox4a	0x000000 0x200000	0x59 0x5a	-0x200000		-0x0000000	0x79	0x000000 0x000000	
		c2b -0x000000		-0x000000		-0x200000	0x5a 0x5b	-0x0000000		-0x0000000		-0x7fffff	
0x0c0x000000 0x	1c0x000000 0x	c2c -0x200000	0x3c	0x000000	0x4c	0x000000	0x5c	0x000000	0x6c ·	-0x000000	0x7c	-Ox7fffff	
		2d -0x000000		-0x000000		0x000000	0x5d	0x000000		-0x200000		-0x7fffff	
		c2e -0x000000 c2f -0x000000		0x000000 0x000000		0x000000 0x200000	0x5e	0x200000 0x000000		0x000000 0x000000		-Ox7fffff -Ox7fffff	
	11 0x000000 0x	21 0X000000	OXJI	02000000	0241	0x200000	OXJI	00000000	OXOL	0x000000	DXIT	OXIIIIII	

D-821Di can use SAVE button to store register values, which will generate one file: user\_defined.txt. This file has two portions. The first portion shows all register values and RAM contents that are read back from D-821Di. This content will be used by the system developer to build audio driver in the system software. The second portion contains all GUI related information.

When the LOAD button is pressed, user\_defined.txt is used by GUI to generate the previously saved register values and RAM contents.

The user\_defined.txt file has the following format (values are in hexadecimal representation).



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```
2 #Product:d820
 3 #Date:2014/02/05
 5
 7 Reg[OOh]=OOh ##Device ID register and Revision register
 8 Reg[01h]=00h ##IF register
9 Reg[02h]=00h ##MUTE CM1 CM2 CM3 register
10 Reg[03h]=10h ##LREXC NG FADE EN DTC EN NG EN register
11 Reg[04h]=00h ##State Control
12 Reg[05h]=11h ##Channel_1_configuration_registers
13 Reg[06h]=11h ##Channel_2_configuration_registers
14 Reg[07h]=11h ##Channel_3_configuration_registers
15 Reg[08h]=11h ##Channel 4 configuration registers
16 Reg[09h]=80h ##HVUV_EN_HV_UVSEL_LV_UVSEL_register
17 Reg[OAh]=80h ##DTC_TH_DTC_RATE_register
18 Reg[OBh]=OOh ##ERROR delay register
19 Reg[OCh]=08h ##Protection_circuit_register
20 Reg[ODh]=OOh ##Memory BIST register
21 Reg[OEh]=feh ##ERROR_Status_register
22 Reg[OFh]=00h ##PWM_control_register
23 Reg[10h]=00h ##Test Mode register
24 Reg[11h]=00h ##Volume FT register
25 Reg[12h]=00h ##C4V FT register
26 Reg[13h]=Och ##MV register
27 Reg[14h]=Och ##C1V_register
28 Reg[15h]=Och ##C2V_register
29 Reg[16h]=Och ##C3V register
30 Reg[17h]=Och ##C4V_register
31 Reg[18h]=6ah ##LA1 and LR1 register
```

#### 6.4 Load

D-821Di can use LOAD button to load user\_defined.txt to program the previously saved

register and RAM values.

Address [Value 0f.         Address           0x00         -0x00         0x10           0x11         -0x00         0x11           0x02         -0x00         0x12           0x03         -0x10         0x10           0x10         -0x00         0x12           0x02         -0x10         0x13           0x04         -0x00         0x14           0x05         -0x11         0x15           0x06         -0x11         0x15           0x06         -0x11         0x16           0x07         -0x11         0x16           0x08         -0x10         0x19           0x0a         -0x80         0x19	tetr Table         Address [Value 0];           0.000         0.020         -0.000           -0000         0.020         -0.000           -0000         0.021         -0.000           -0000         0.022         -0.000           -0000         0.022         -0.000           -0000         0.023         -0.000           -0000         0.025         -0.000           -0000         0.025         -0.000           -0.000         0.027         -0.000	Read Register Table Address: 0x20 to 0x27 Address: 0x20 to 0x57 Address: 0x20 to 0x57 Read RAM Address: 0x50 to 0x77 Address: 0x50 to 0x77	
0x000x08         0x1e           0x04 - 0x00         0x1e           0x0e0x7e         0x1e           0x0f0x7e         0x1e           0x0f - 0x10         0x1f	-0x00 -0	總統編 (C.) マーク C で E の SK Strup の SK Strup の WINDOWS の Killinx 日本 1000	Value 00         Address [Value 00]           >         >           >         >           >         >           >         >
$ \begin{array}{cccccccccccccccccccccccccccccccccccc$	2000000 は000000         株家装着型(力):         州y Dut 5000000           1000000         b,25         -0±00000         b,33           1000000         b,27         -0±00000         b,33           1000000         b,27         -0±00000         b,33           1000000         b,22         -0±000000         b,33	BEA (*5x)         N           -0x200000         0x46         -0x00000         0x56         -0x00000           -0x00000         0x48         -0x00000         0x57         -0x00000           -0x00000         0x48         -0x00000         0x59         -0x00000           -0x00000         0x48         -0x00000         0x59         -0x00000           -0x00000         0x44         -0x00000         0x54         -0x00000           -0x00000         0x44         -0x00000         0x54         -0x00000           -0x44         -0x00000         0x54         -0x000000         0x54<	№         №



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### 7. "Headphone" Page

#### 7.1 Head Phone AMP Control

HeadPhone AMI	P Control
HP_EN_L	Disable 💌
HP_EN_R	Disable 💌
HP_MUTE_L	Disable 💌
HP_MUTE_R	Disable 💌

When enable HP\_EN\_L or HP\_EN\_R function, the LCH or RCH of headphone will enable. When enable HP\_MUTE\_L or HP\_ MUTE \_R function, the LCH or RCH of headphone will be mute.

#### 7.2 Head Phone Volume Control

HP_Volume	 0.00

Head phone volume control ranges from 0dB to +24dB with .25dB increment. The volume for headphone shown in the above box.



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NOTICE The

The information provided is preliminary, and subject to change without notice. Please check for the latest information when using this product in your design.

	——— Y/	AMAHA CORPORATION ——					
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