2x5W Stereo / 1x10W Mono Class-D Audio Amplifier With Built-in Step-up Converter

Features

- Input voltage 2.6V~5.5V
- Adjustable boost converter output up to 9V
- Adjustable over current protection: 0.5A~4.5A
- Loudspeaker power from 9V supply @V_{CC}=5V
  Stereo: 5W/CH into 8Ω @ <10% THD+N
  Mono (PBTL): 10W/CH into 4Ω @THD+N=10%
- Loudspeaker power from 8V supply @V_{CC}=3.6V
  Stereo: 4W/CH into 8Ω @ <10% THD+N
  Mono (PBTL): 8W/CH into 4Ω @ THD+N=10%
  Mono (PBTL): 7W/CH into 4Ω @ THD+N=1%
- Differential inputs signal
- Four selectable, fixed gain settings
- Internal oscillator
- Short-Circuit protection with auto recovery option
- Under-Voltage detection
- Over-Voltage protection
- Pop noise and click noise reduction
- Adjustable power limit function for speaker protection
- Output DC detection for speaker protection
- Filter-Free operation
- Over temperature protection with auto recovery
- Superior EMC performance

Applications

- Blue-tooth Box
- Portable Media
- Audio Docking System
- Tablet Personal PC
- Consumer Audio Equipment

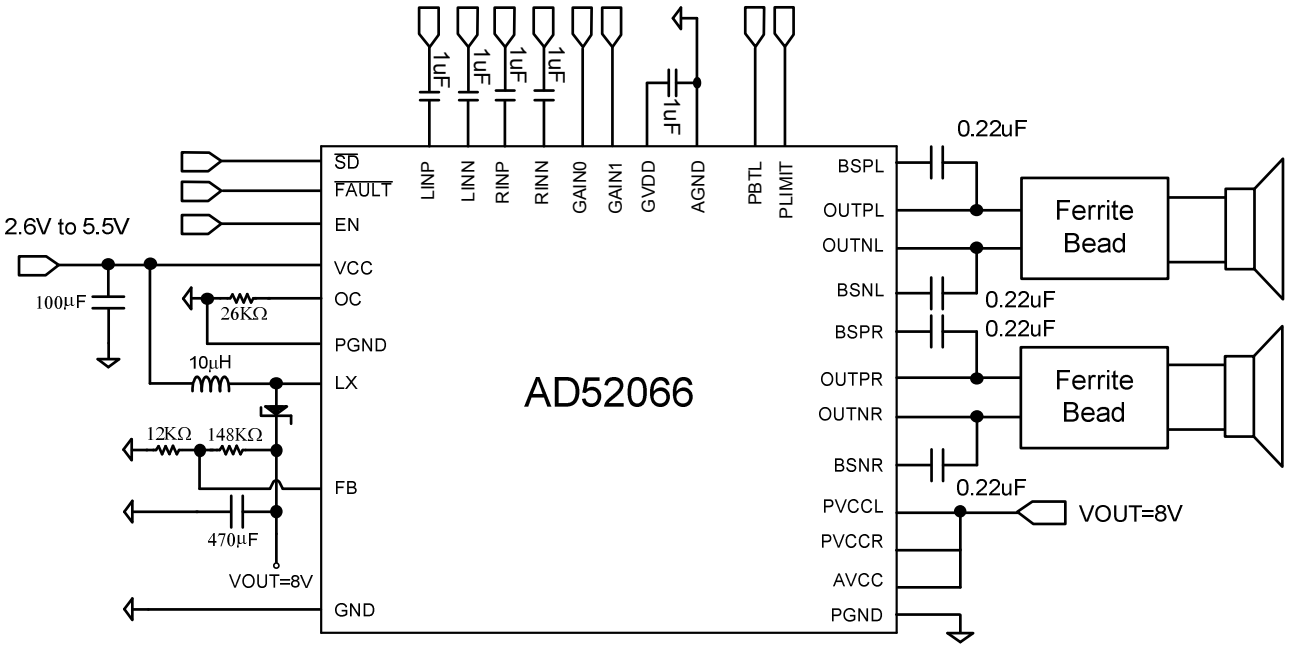
Description

The AD52066 is a high efficiency stereo class-D audio amplifier with built-in boost DC-DC converter. The loudspeaker driver can deliver 5W/CH output power into 8Ω loudspeaker within 10% THD+N at 5V supply voltage; driver 4W/CHx2 output power into 8Ω loudspeaker within 10% THD+N at Li-ion battery.

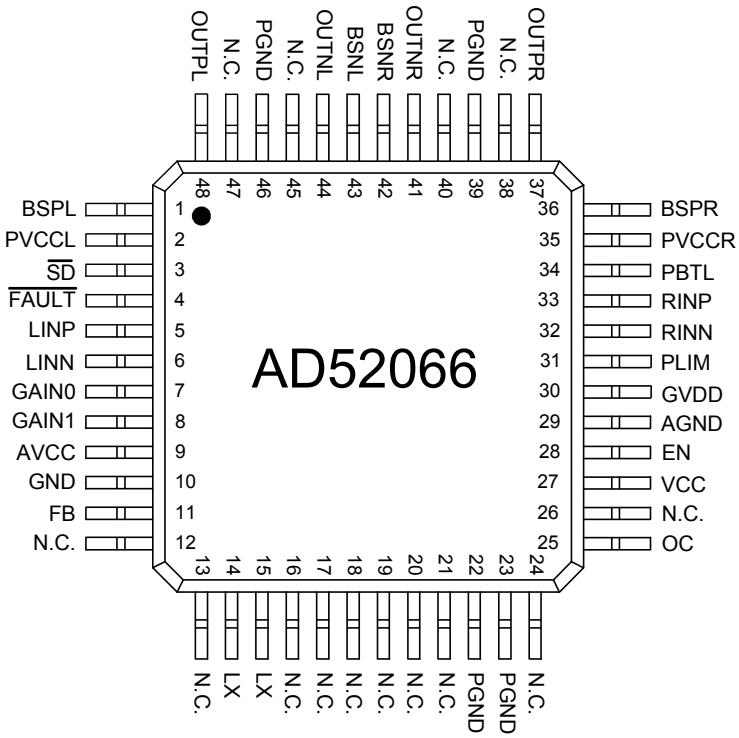
AD52066 provides parallel BTL (Mono) application also, and it can deliver 10W into 4Ω loudspeaker at 5V supply voltage. The adjustable power limit function allows user to set a voltage rail lower than half of 5V to limit the amount of current through the speaker.

Output DC detection prevents speaker damage from long-time current stress. AD52066 provides superior EMC performance for filter-free application. The output short circuit and over temperature protection include auto-recovery feature.

Simplified Application Circuit



Pin Assignments



Pin Description

NAME	E-LQFP-48L	TYP	DESCRIPTION
BSPL	1	I	Bootstrap I/O for left channel, positive high side FET.
PVCCL	2	P	High-voltage power supply for left-channel. Right channel and left channel power supply inputs are connect internal.
$\overline{SD}$	3	I	Shutdown signal for IC (low = disabled, high = operational). Voltage compliance to AVCC.
$\overline{FAULT}$	4	O	Open drain output used to display short circuit or dc detect fault. Voltage compliant to AVCC. Short circuit faults can be set to auto-recovery by connecting FAULTB pin to $\overline{SD}$ pin. Otherwise, both short circuit faults and dc detect faults must be reset by cycling AVCC.
LINP	5	I	Positive audio input for left channel. Biased at 2.5V.
LINN	6	I	Negative audio input for left channel. Biased at 2.5V.
GAIN0	7	I	Gain select least significant bit. Voltage compliance to AVCC.
GAIN1	8	I	Gain select least significant bit. Voltage compliance to AVCC.
AVCC	9	P	Analog supply.
GND	10	P	Boost ground pin
FB	11	I	Receives the feedback voltage from an external resistive divider across the output.
N.C.	12		Not connected.
N.C.	13		Not connected.

LX	14,15	O	Must be connected an Inductor from VCC pin to LX pin for boost and rectifying switches.
N.C.	16,17,18 ,19,20,21		Not connected.
PGND	22,23	P	Power Switch Ground Pin.
N.C.	24		Not connected.
OC	25	I	OC adjustable via a resister from OC pin to GND (floating available).
N.C.	26	O	Not connected.
VCC	27	P	Must be closely decoupled to GND pin with 470uF*1or greater ceramic capacitor.
EN	28	I	Boost enable pin (low=Enable; high=Disable).
AGND	29	P	Analog signal ground. Connect to the thermal pad.
GVDD	30	O	5V regulated output, also used as supply for PLIMIT function.
PLIM	31	I	Power limit level adjustment. Connect a resistor divider from GVDD to GND to set power limit. Give V(PLIMIT) <2.4V to set power limit level. Connect to GVDD (>2.4V) or GND to disable power limit function.
RINN	32	I	Negative audio input for right channel. Biased at 2.5V.
RINP	33	I	Positive audio input for right channel. Biased at 2.5V.
PBTL	34	I	Parallel BTL mode switch, high for parallel BTL output. Voltage compliance to AVCC.
PVCCR	35	P	High-voltage power supply for right-channel. Right channel and left channel power supply inputs are connect internal.
BSPR	36	I	Bootstrap I/O for right channel, positive high side FET.
OUTPR	37	O	Class-D H-bridge positive output for right channel.
N.C.	38		Not connected.
PGND	39	P	Power ground for the H-bridges.
N.C.	40		Not connected.
OUTNR	41	O	Class-D H-bridge negative output for right channel.
BSNR	42	I	Bootstrap I/O for right channel, negative high side FET.
BSNL	43	I	Bootstrap I/O for left channel, negative high side FET.
OUTNL	44	O	Class-D H-bridge negative output for left channel.
N.C.	45		Not connected.
PGND	46	P	Power ground for the H-bridges.
N.C.	47		Not connected.
OUTPL	48	O	Class-D H-bridge positive output for left channel.
Thermal Pad		P	Must be soldered to PCB's ground plane.

Note:

P: Power or ground pins; I: Input pins; O: Output pins; I/O: The bidirectional pins

Ordering Information

Product ID	Package	Packing / MPQ	Comments
AD52066-LG48NRY	E-LQFP-48L 7X7	250Units / Tube 2.5K Units / Box(10 Tray)	Green

Available Package

Package Type	Device No.	θ_{ja}(℃/W)	θ_{jt} (℃/W)	Ψ_{jt} (℃/W)	Exposed Thermal Pad
E-LQFP-48L 7X7	AD52066	22.9	34.9	1.64	Yes (Note1)

Note 1.1: The thermal pad is located at the bottom of the package. To optimize thermal performance, soldering the thermal pad to the PCB's ground plane is suggested.

Note 1.2: θ_{ja} is measured on a room temperature (T_A=25℃), natural convection environment test board, which is constructed with a thermally efficient, 4-layers PCB (2S2P). The measurement is tested using the JEDEC51-5 thermal measurement standard.

Note 1.3: θ_{jt} represents the heat resistance for the heat flow between the chip and the package's top surface. (The junction-to-top thermal resistance is obtained by simulating a cold plate test on the top of the package).

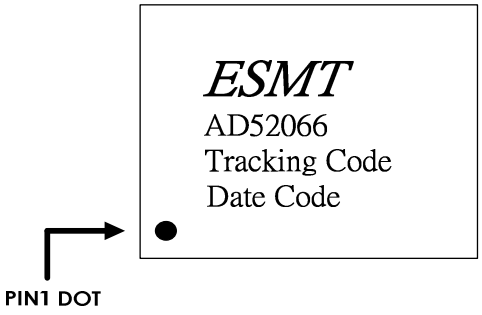
Note 1.4: Ψ_{jt} represents the heat resistance for the heat flow between the chip and the exposed pad center. (The junction-to-top characterization parameter is extracted from the simulation data to obtain θ_{ja}).

Marking Information

AD52066

- Marking Information

Line 1：LOGO
Line 2：Product No
Line 3：Tracking Code
Line 4：Date Code



Absolute Maximum Ratings

Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
VCC	Supply voltage	VCC	-0.3	6	V
$V_{I(boost)}$	Interface pin voltage for boost	EN, FB	-0.3	VCC	V
	Boost switch pin	LX	-0.3	12	V
PVCC	Class-D supply voltage	PVCCL, PVCCR, AVCC	-0.3	12	V
$V_{I(Class-D)}$	Interface pin voltage	$\overline{SD}$, GAIN0, GAIN1, PBTL, $\overline{FAULT}$,	-0.3	12	V
		PLIMIT	-0.3	5.5	
T_A	Operating free-air temperature range		-40	85	°C
T_J	Operating junction temperature range		-40	150	°C
T_{stg}	Storage temperature range		-65	150	°C
R_L	Minimum Load Resistance	BTL, PBTL	3.2		Ω

Recommended Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
VCC	Supply voltage	VCC	2.6	5.5	V
PVCC	Class-D supply voltage	PVCCL, PVCCR, AVCC	4.5	9	V
V_{IH}	High-level input voltage	$\overline{SD}$, GAIN0, GAIN1, PBTL, EN	2		V
V_{IL}	Low-level input voltage	$\overline{SD}$, GAIN0, GAIN1, PBTL, EN		0.6	V
V_{OL}	Low-level output voltage	FAULT, $R_{PULL-UP}$=100k, V_{CC}=8V		0.8	V
T_A	Operating free-air		-40	85	°C

Boost General Electrical Characteristics

- VCC=4.2, PVCC=8V, T_A=25°C (unless otherwise noted)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	Input Supply Range		2.6		5.5	V
V_{UVLO}	Under Voltage Lockout			2.2		V
	UVLO Hysteresis			0.1		V
F_{OSC}	Operation Frequency	V_{FB}=1.0V	400	500	600	kH_Z
△f / △V	Frequency Change with Voltage	V_{CC}=2.6V to 5.5V		5		%
T_{DUTY}	Maximum Duty Cycle			90		%
V_{REF}	Reference Voltage		0.588	0.6	0.612	V
V_{EN}	Enable Voltage		0.96			V
V_{EN}	Shutdown Voltage				0.6	V
$R_{DS\ (ON)}$	On Resistance of Driver	I_{LX}=2A		80		mΩ
I_{OCP}	Adjustable OCP Current	With External Resistor：26k~500kΩ	0.5		4.5	A

Audio General Electrical Characteristics

- PVCC=8V, R_L=8Ω, T_A=25°C (unless otherwise noted)

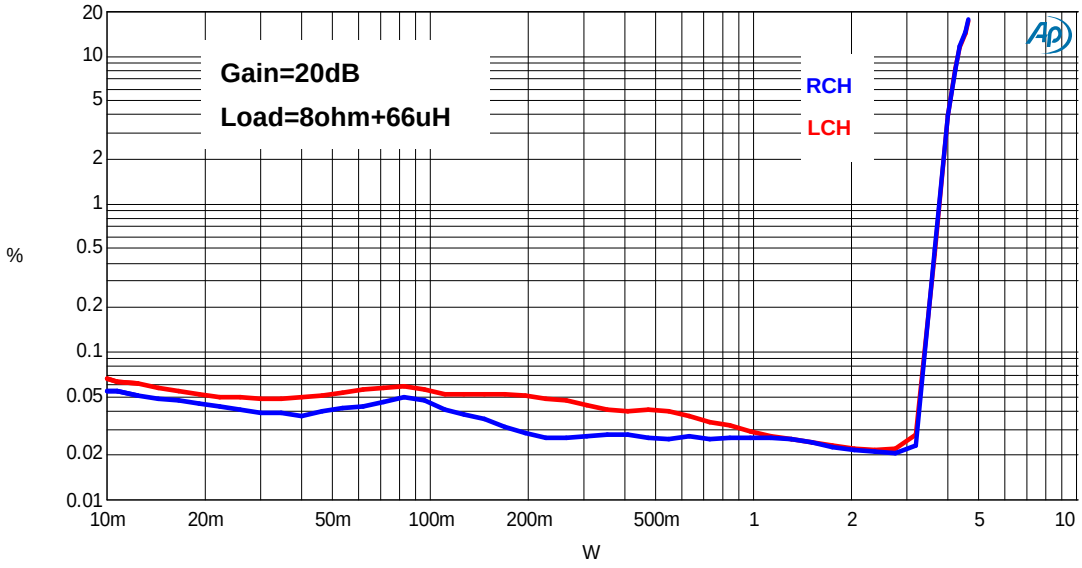
SYMBOL	PARAMETER	CONDITION		MIN	TYP	MAX	UNIT
$R_{DS(on)}$	Drain-source on-state resistance-High side NMOS	PVCC=8V, Id=250mA, T_J=25 °C			220		mΩ
	Drain-source on-state resistance-Low side NMOS				220		mΩ
$\|V_{OS}\|$	Class-D output offset voltage (measured differential)	PVCC=8V V_I=0V, Gain=36dB			1.5	15	mV
t_{ON}	Turn-on time	SD=2V			90		ms
t_{OFF}	Turn-off time	SD=0.8V			2		μs
GVDD	Regulator output	I_{GVDD}=0.1mA		4.75	5	5.25	V
G	Gain	GAIN1 =0.8V	GAIN0=0.8V	18	20	22	dB
			GAIN0=2V	24	26	28	
		GAIN1 =2V	GAIN0=0.8V	30	32	34	
			GAIN0=2V	34	36	38	

Electrical Characteristics and Specifications of Loudspeaker Driver

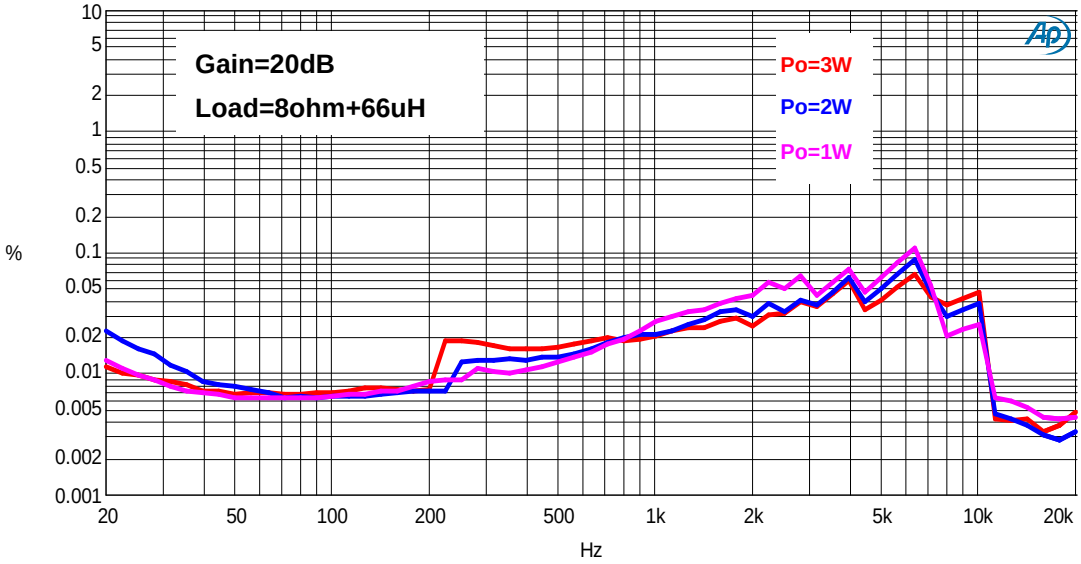
- VCC=4.2V, PVCC=8V, R_L=8Ω, T_A=25°C (unless otherwise noted)

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
P_O	Output power	THD+N=1%, f=1kHz, PVCC=8V		3.7		W
		THD+N=10%, f=1kHz, PVCC=8V		4.2		
THD+N	Total harmonic distortion plus noise	PVCC=8V, R_L=8Ω, f=1kHz, P_O=3W		0.02		%
		PVCC=8V, R_L=8Ω, f=1kHz, P_O=2W		0.02		
SNR	Signal to noise ratio	Maximum output at THD+N<1%, f=1kHz, Gain=20dB, a-weighted		95		dB
V_n	Output integrated noise	F=20Hz ~ 20kHz, Gain=20dB, a-weighted filter, R_L=8Ω		95		μV
K_{SVR}	Power Supply Rejection Ratio	V_{ripple}=200mVpp at 1kHz, Gain=20dB, inputs ac-grounded		-70		dB
Crosstalk	Crosstalk	F=1kHz, V_O=1Vrms, Gain=20dB		-102		dB
Quiescent Current	Iq	VCC=4.2V, PVCC=8V		42		mA
Shutdown Current	Isd	VCC=4.2V, PVCC=8V		32		uA
f_{OSC}	Oscillator frequency		250	310	370	kHz
T_{SENSOR}	Thermal trip point			150		°C
	Thermal hysteresis			25		°C

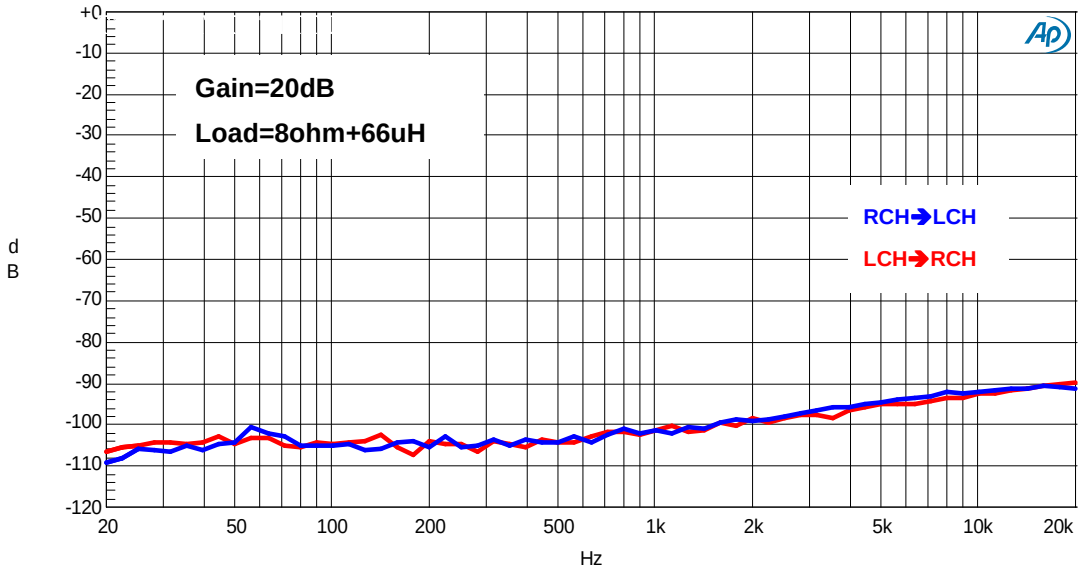
THD + N (%) vs. Output power (8ohm load)



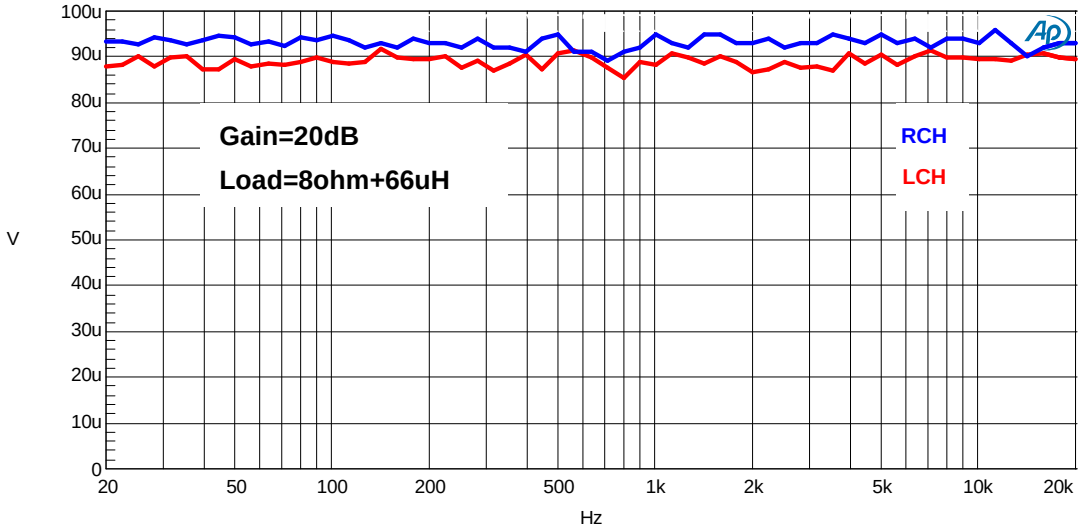
THD + N (%) vs. Frequency



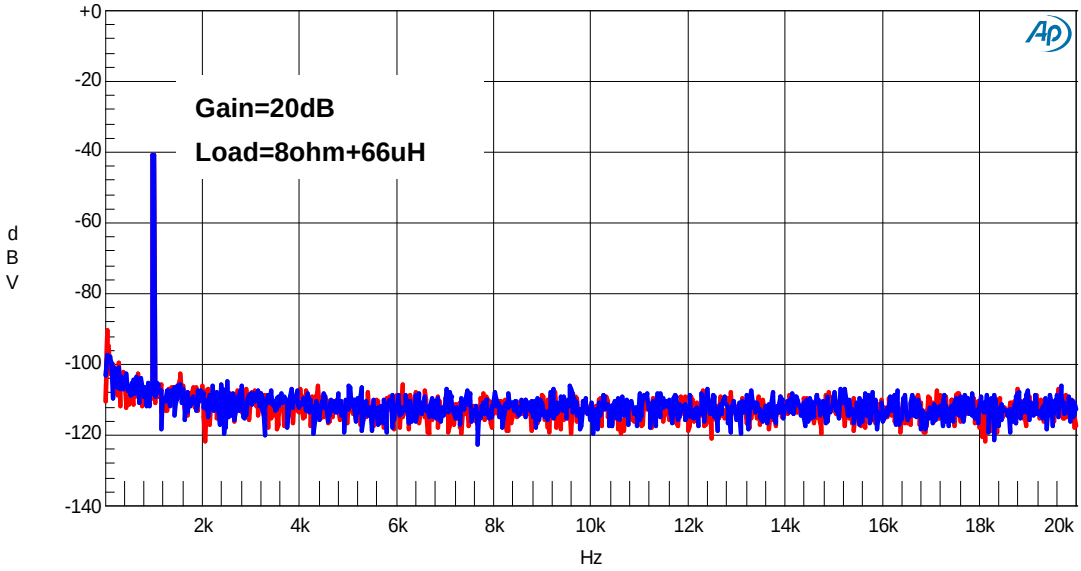
Crosstalk



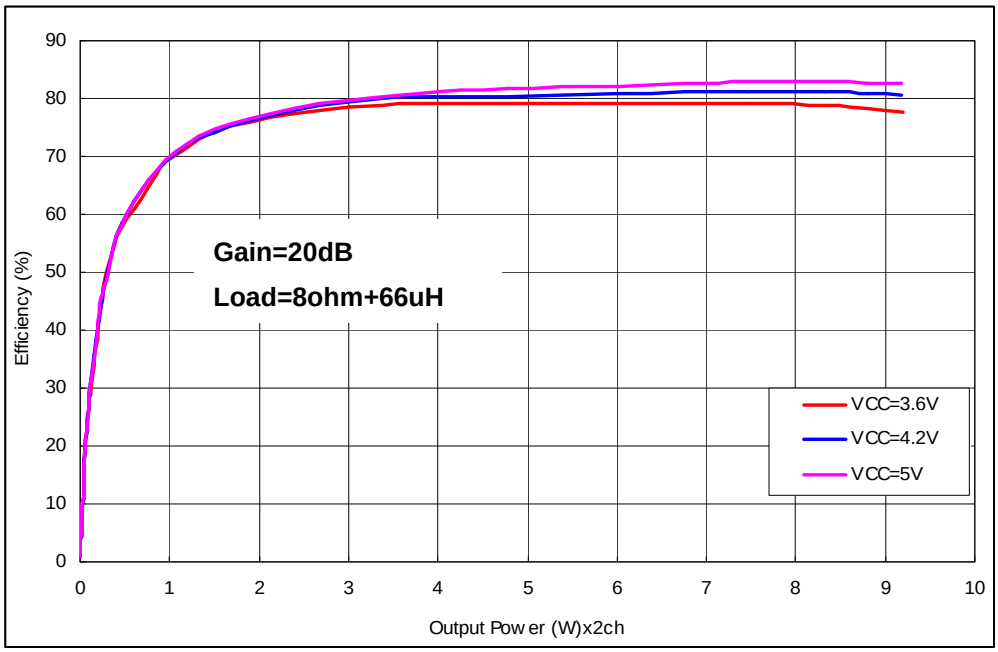
Noise


100u
90u
80u
70u
60u
50u
40u
30u
20u
10u
0
V
Gain=20dB
Load=8ohm+66uH
RCH
LCH
20
50
100
200
500
1k
2k
5k
10k
20k
Hz

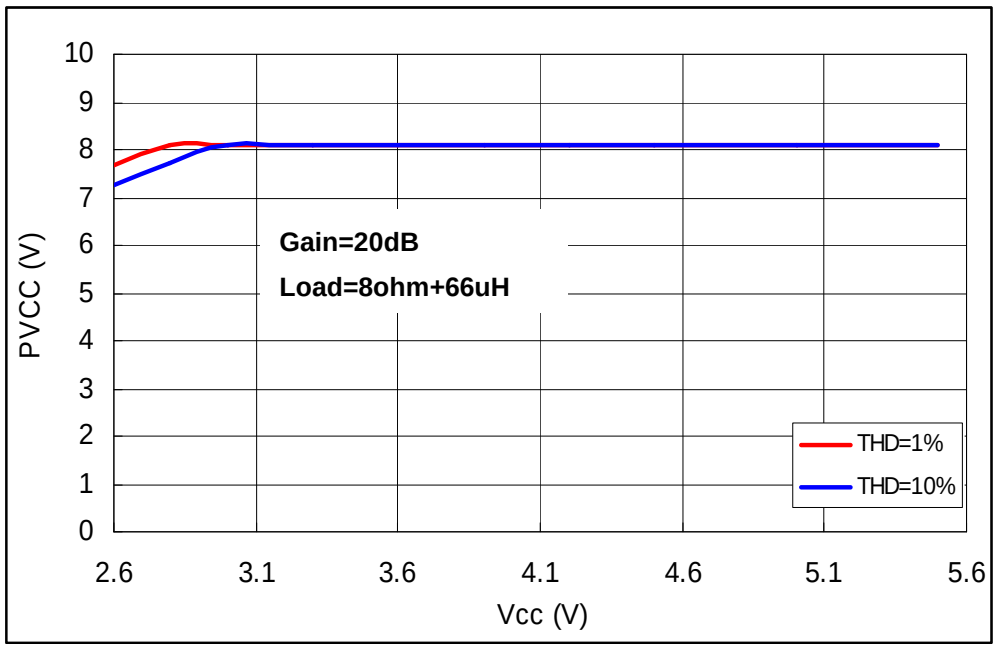
DR


+0
-20
-40
-60
-80
-100
-120
-140
dBV
Gain=20dB
Load=8ohm+66uH
2k
4k
6k
8k
10k
12k
14k
16k
18k
20k
Hz

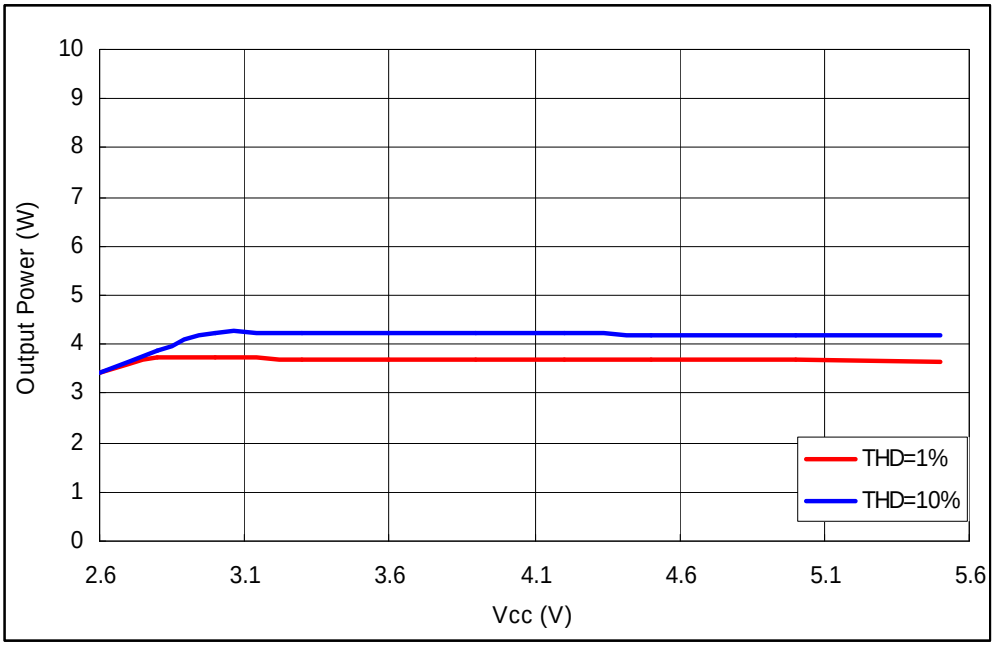
Efficiency (8ohm+66uH load) / 2ch



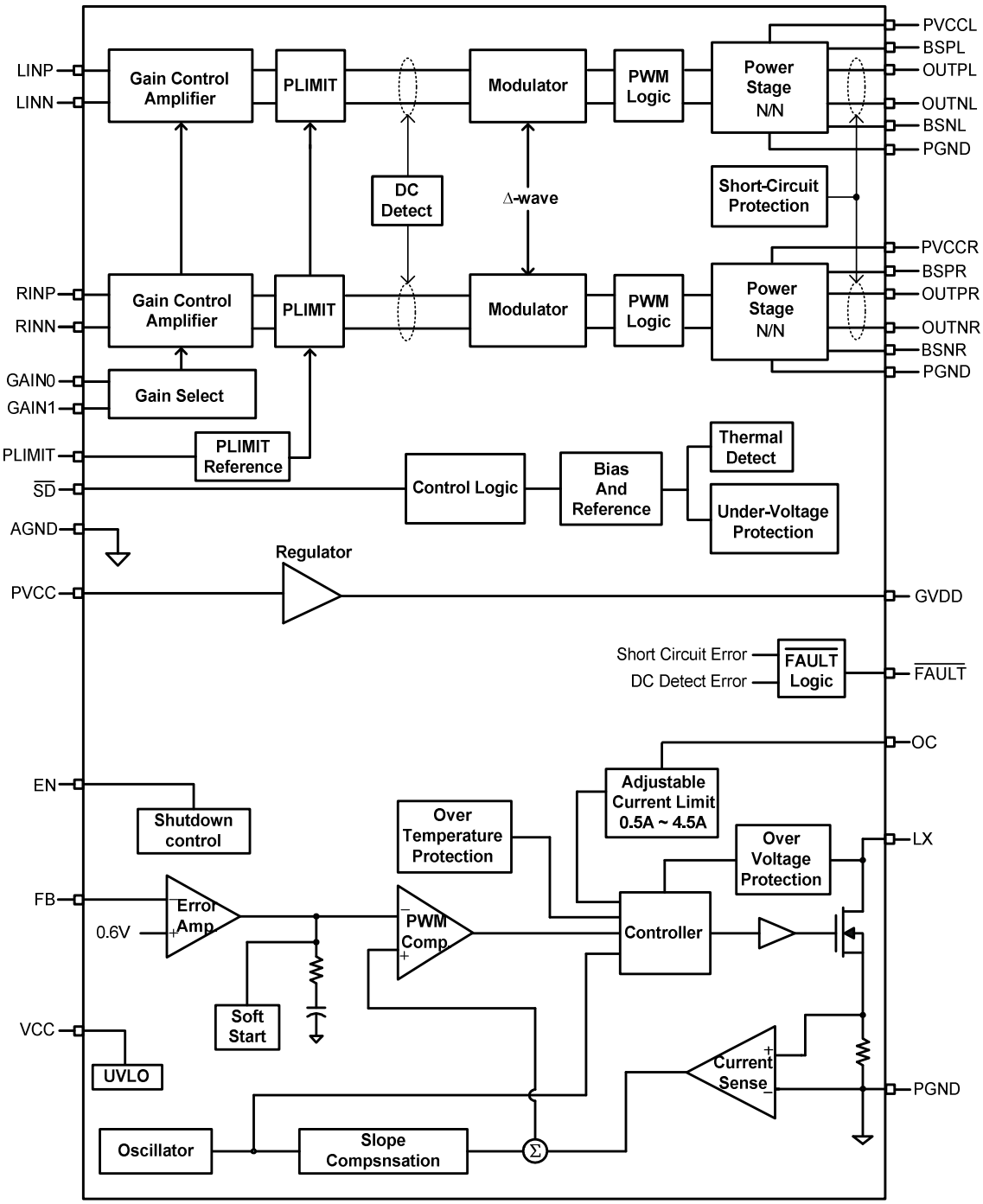
VCC vs. PVCC



VCC vs. Output Power



Functional Block Diagram



Boost Converter Operation Description

- **Detailed Description**

  The AD52066 is a high efficiency stereo class-D audio amplifier with built-in boost dc-dc converter. The constant switching frequency is 500kHz and operates with pulse width modulation (PWM). Build-in 12V / 4.5A MOSFET provides a high output voltage. The control loop architecture is peak current mode control; therefore slope compensation circuit is added to the current signal to allow stable operation for duty cycles larger than 50%.

- **Adjustable Current Limit**

  A resistor between OC and GND pin programs peak switch current. The resistor value should be between 26k and 500kohm. The current limit will be set from 4.5A to 0.5A. Keep traces at this pin as short as possible. Do not put capacitance at this pin. To set the over current trip point according to the following equation,

$$I_{OCP} = \frac{110000}{R3} + 0.3$$

- **Over Voltage Protection**

  In some condition, the resistive divider may be unconnected, which will cause PWM signal to operate with maximum duty cycle and output voltage is boosted higher and higher. The power MOSFET will be turned off immediately, when the output voltage exceeds the OVP threshold level. The AD52066's OVP threshold is 12V.

- **Soft Start**

  Soft start circuitry is integrated into AD52066 to avoid inrush current during power on. After the IC is enabled, the output of error amplifier is clamped by the internal soft-start function, which causes PWM pulse width increasing slowly and thus reducing input surge current.

Audio Operation Description

- **Gain settings**

  The gain of the AD52066 is set by two input pins, GAIN0 and GAIN1. By varying input resistance in AD52066, the various volume gains are achieved. The respective volume gain and input resistance are listed in Table 1. However, there is 20% variation in input resistance from production variation.

Table 1. Volume gain and input impedance

GAIN1	GAIN0	Volume Gain (dB)	Input Resistance, R_{in} (kΩ)
0	0	20	60
0	1	26	30
1	0	32	15
1	1	36	9

- **Shutdown ($\overline{SD}$) control**

  Pulling $\overline{SD}$ pin low will let AD52066 operate in low-current state for power conservation. The AD52066 outputs will enter mute once $\overline{SD}$ pin is pulled low, and regulator will also disable to save power. If let $\overline{SD}$ pin floating, the chip will enter shutdown mode because of the internal pull low resistor. For the best power-off performance, place the chip in the shutdown mode in advance of removing the power supply.

- **DC detection**

  AD52066 has dc detection circuit to protect the speakers from DC current which might be occurred as input capacitor defect or inputs short on printed circuit board. The detection circuit detects first volume amplifier stage output, when both differential outputs' voltage become higher than a determined voltage or lower than a determined voltage for more than 420ms, the dc detect error will occur and report to $\overline{FAULT}$ pin. At the same time, loudspeaker drivers of right/left channel will disable and enter Hi-Z. This fault can not be cleared by cycling $\overline{SD}$, it is necessary to cycle the PVCC supply.

  The minimum differential input voltages required to trigger the DC detect function are shown in table2. The input voltage must keep above the voltage listed in the table for more than 420msec to trigger the DC detect fault. The equivalent class-D output duty of the DC detect threshold is listed in table3.

Table 2. DC Detect Threshold

AV (dB)	Vin (mV, differential)
20	250
26	125
32	63
36	35

Table 3. Output DC Detect Duty (for Either Channel)

PVCC (V)	Output Duty Exceeds
8	20.8%

- **Thermal protection**

  If the internal junction temperature is higher than 150°C, the outputs of loudspeaker drivers will be disabled and at low state. The temperature for AD52066 returning to normal operation is about 125°C. The variation of protected temperature is about 10%. Thermal protection faults are NOT reported on the $\overline{\text{FAULT}}$ pin.

- **Short-circuit protection**

  To protect loudspeaker drivers from over-current damage, AD52066 has built-in short-circuit protection circuit. When the wires connected to loudspeakers are shorted to each other or shorted to PGND or to PVCC, overload detectors may activate. Once one of right and left channel overload detectors are active, the amplifier outputs will enter a Hi-Z state and the protection latch is engaged. The short protection fault is reported on $\overline{\text{FAULT}}$ pin as a low state. The latch can be cleared by reset $\overline{\text{SD}}$ or power supply cycling.

  The short circuit protection latch can have auto-recovery function by connect the $\overline{\text{FAULT}}$ pin directly to $\overline{\text{SD}}$ pin. The latch state will be released after 420msec, and the short protection latch will re-cycle if output overload is detected again.

- **Under-voltage detection**

  When the GVDD voltage is lower than 2.8V or the PVCC voltage is lower than 4V, loudspeaker drivers of right/left channel will be disabled and kept at low state. Otherwise, AD52066 return to normal operation.

- **Power limit function**

  - The voltage at PLIMIT pin can used to limit the power of first gain control amplifier output. Add a resistor divider from GVDD to ground to set the voltage V_{PLIMIT} at the PLIMIT pin. The voltage V_{PLIMIT} sets a limit on the output peak-to-peak voltage. PLIMIT is adjustable from 1.33V~2.5V.

  For normal BTL operation (Stereo) and PBTL (Mono) operation:

  $$P_{OUT-LIMIT} = \{[(2.51 - V_{PLIMIT})/2.88] \times 2 \times PVDD\}^2 / (2 \times RL)$$

  Connect PLIMIT pin to ground or GVDD to disable power limit function.

- **PBTL (Mono) function**

  AD52066 provides the application of parallel BTL operation with two outputs of each channel connected directly. If the PBTL pin is tied high, the positive and negative outputs of left and right channel are synchronized and in phase. Apply the input signal to the RIGHT channel input in PBTL mode and let the LEFT channel input grounded, and place the speaker between the LEFT and RIGHT outputs. The output swing is doubled of that in normal mode. See the application circuit example for PBTL (Mono) mode operation. For normal BTL (Stereo) operation, connect the PBTL pin to ground.

Boost Converter Application information

- **Inductor Selection**

  Inductance value is decided based on different condition. 6.8uH to 10µH inductor value is recommended for general application circuit. There are three important inductor specifications, DC resistance, saturation current and core loss. Low DC resistance has better power efficiency.

- **Capacitor Selection**

  The output capacitor is required to maintain the DC voltage. Low ESR capacitors are preferred to reduce the output voltage ripple. Ceramic capacitor of X5R and X7R are recommended, which have low equivalent series resistance (ESR) and wider operation temperature range.

- **Diode Selection**

  Schottky diodes with fast recovery times and low forward voltages are recommended. Ensure the diode average and peak current rating exceed the average output current and peak inductor current. In addition, the diode's reverse breakdown voltage must exceed the output voltage.

- **Output Voltage Setting**

  The output voltage of AD52066 can be adjusted by a resistive divider according to the following formula:

$$V_{OUT} = V_{REF} * \left(1 + \frac{R_1}{R_2}\right) = 0.6 * \left(1 + \frac{R_1}{R_2}\right)$$

The resistive divider senses the fraction of the output voltage as shown in Figure.1 Using large feedback resistor can increase efficiency, but too large value affects the device's output accuracy because of leakage current going into device's FB pin. The recommended value for R2 is therefore in the range of 10~20KΩ.

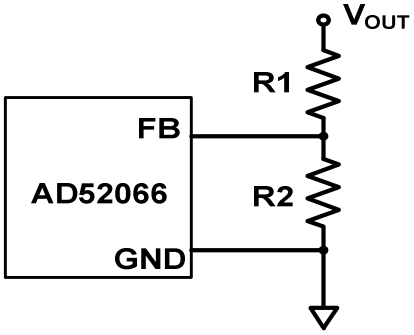


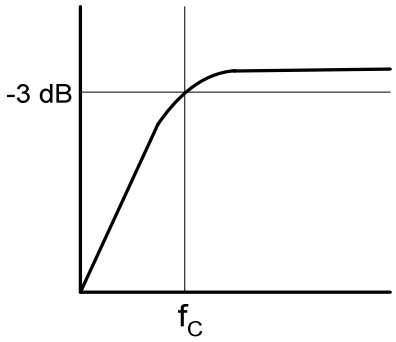
Figure.1 The resistive divider senses the fraction of the output voltage

Audio Application information

- **Input capacitors (C_{in})**

  The performance at low frequency (bass) is affected by the corner frequency (f_c) of the high-pass filter composed of input resistor (R_{in}) and input capacitor (C_{in}), determined in equation (2). Typically, a 0.1μF or 1μF ceramic capacitor is suggested for C_{in}. The resistance of input resistors is different at different gain setting. The respective gain and input resistance are listed in Table 1 (shown at GAIN SETTING). However, there is 20% variation in input resistance from production variation.

$$f_c = \frac{1}{2\pi R_{in} C_{in}} \ (\text{Hz}) \quad \cdots\cdots\cdots (2)$$



- **Ferrite Bead selection**

  If the traces from the AD52066 to speaker are short, the ferrite bead filters can reduce the high frequency emissions to meet FCC requirements. A ferrite bead that has very low impedance at low frequency and high impedance at high frequency (above 1MHz) is recommended. The impedance of the ferrite bead can be used along with a small capacitor with a value around 1000pF to reduce the frequency spectrum of the signal to an acceptable level.

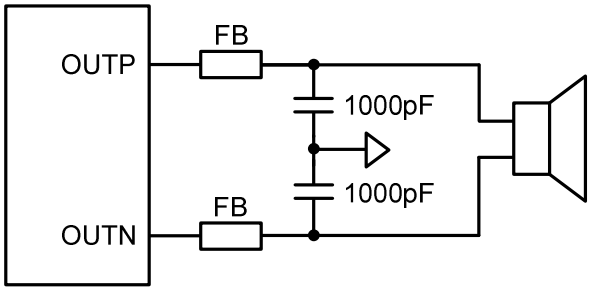


Figure 2. Typical Ferrite Bead Filter

- **Output LC Filter**

  If the traces from the AD52066 to speaker are not short, it is recommended to add the output LC filter to eliminate the high frequency emissions. Figure 3 shows the typical output filter for 8Ω speaker with a cut-off frequency of 27 kHz and Figure 4 shows the typical output filter for 4Ω speaker with a cut-off frequency of 27 kHz.

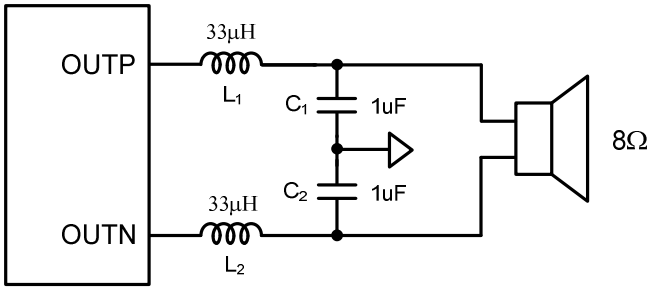


Figure 3. Typical LC Output Filter for 8Ω Speaker

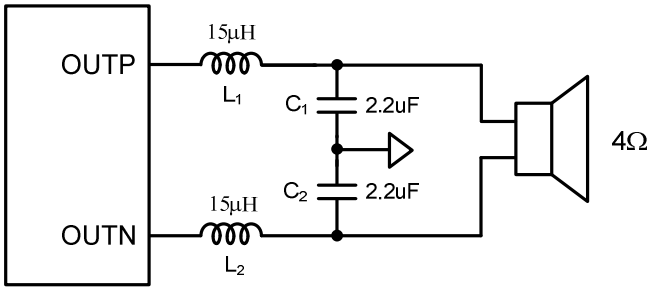


Figure 4. Typical LC Output Filter for 4Ω Speaker

- **Power supply decoupling capacitor (Cs)**

  Because of the power loss on the trace between the device and decoupling capacitor, the decoupling capacitor should be placed close to PVCC and PGND to reduce any parasitic resistor or inductor. A low ESR ceramic capacitor, typically 1000pF, is suggested for high frequency noise rejection. For mid-frequency noise filtering, place a capacitor typically 0.1µF or 1µF as close as possible to the device PVCC leads works best. For low frequency noise filtering, a 100µF or greater capacitor (tantalum or electrolytic type) is suggested.

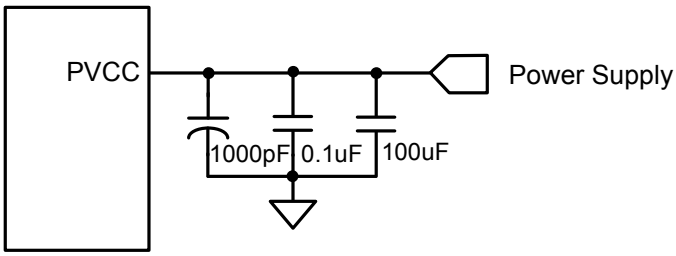
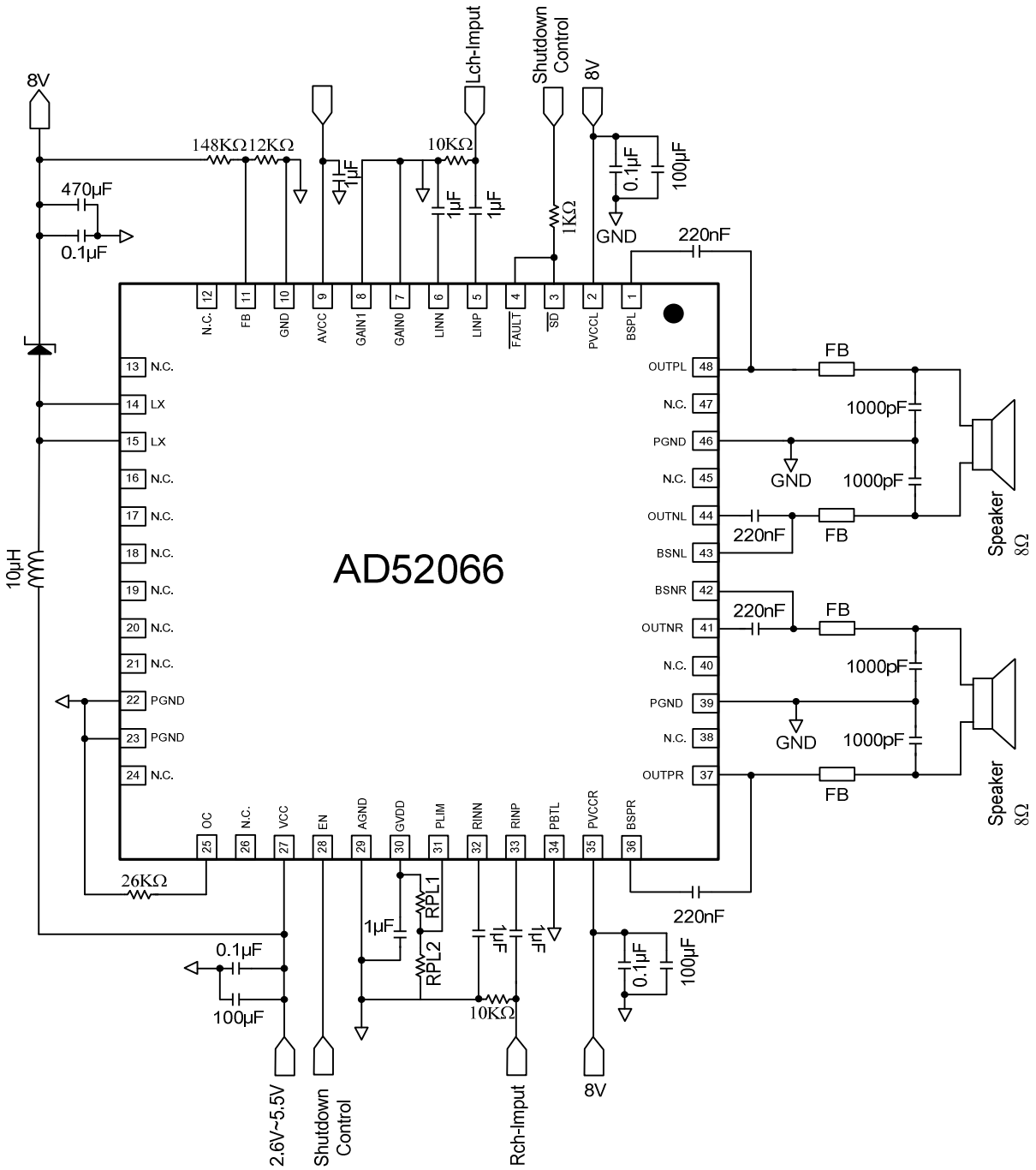


Figure 5. Recommended Power Supply Decoupling Capacitors.

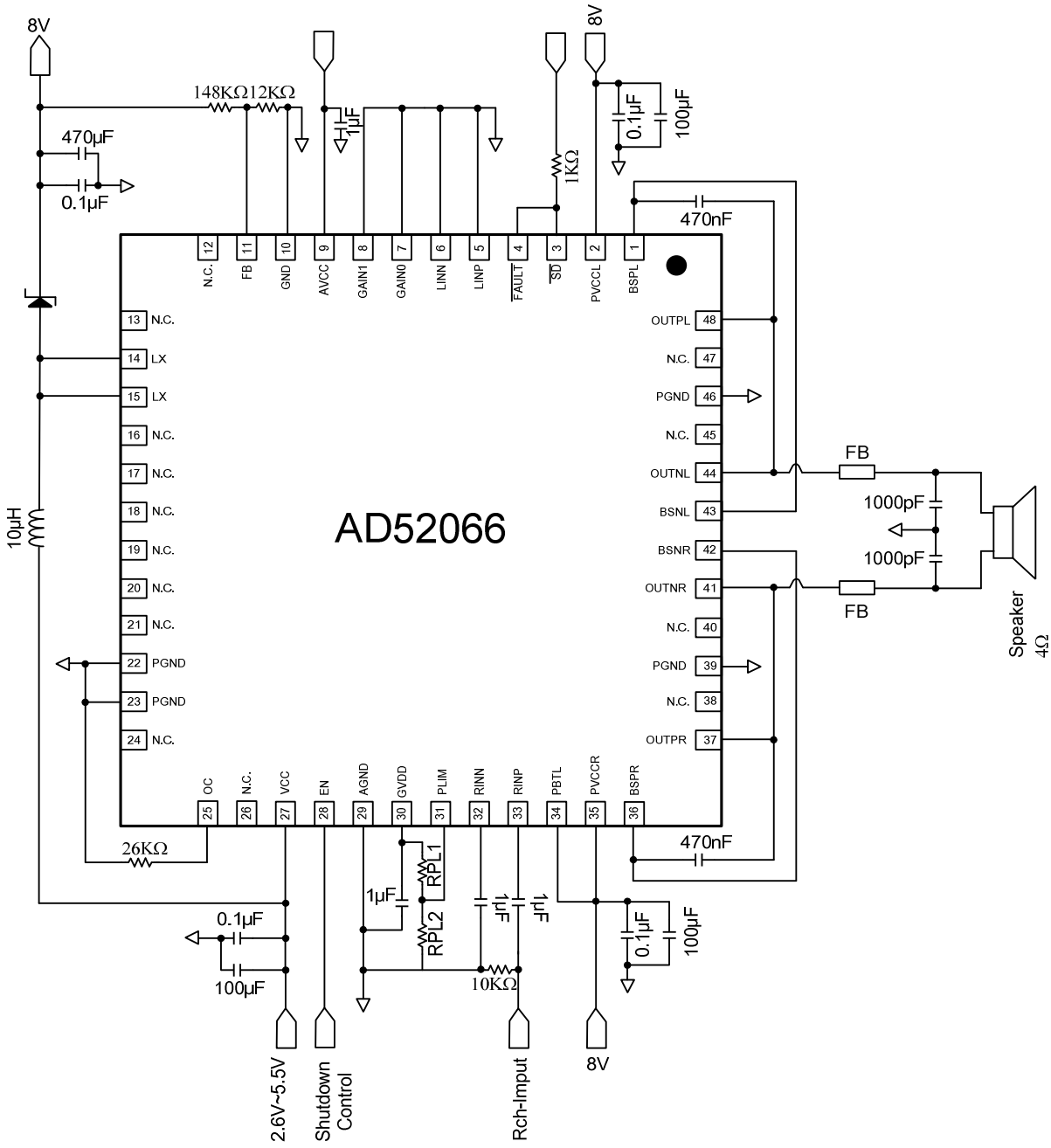
Application Circuit Example

- Application circuit for Stereo (BTL) mode configuration and Singe-Ended Input



Application Circuit Example

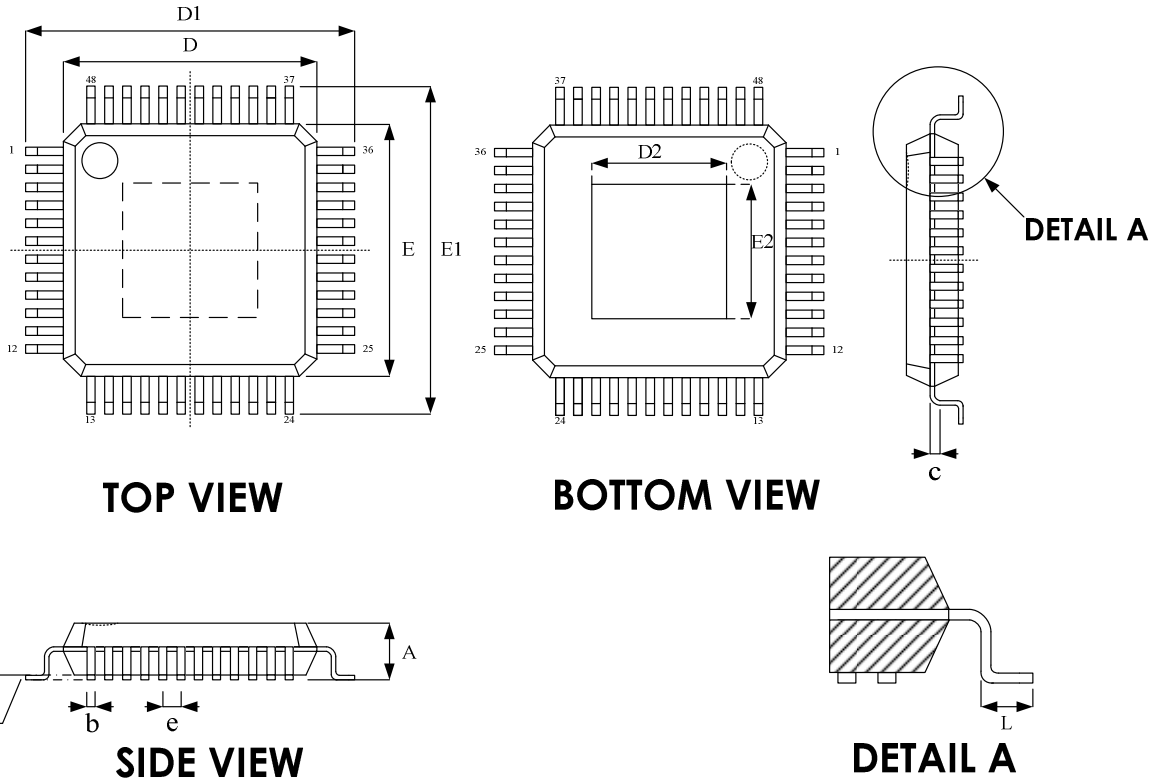
- Application circuit for Mono (parallel BTL) mode configuration and Singe-Ended Input



Note: Be noted that input should be applied on R-channel only for Mono application.

Package Dimensions

- **E-LQFP 48L (7x7mm)**



Symbol	Dimension in mm	
	Min	Max
A	--	1.60
A1	0.05	0.15
b	0.17	0.27
c	0.09	0.20
D	6.90	7.10
D1	8.90	9.10
E	6.90	7.10
E1	8.90	9.10
e	0.50 BSC	
L	0.45	0.75

Exposed pad

	Dimension in mm	
	Min	Max
D2	4.31	5.21
E2	4.31	5.21

Revision History

Revision	Date	Description
0.01	2015.11.19	Draft version.
0.02	2015.11.20	Added Po at THD+N=1% for Mono mode.

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