YMU836

Application Manual

AVP-2 Automotive Voice Processor Type 2

YAMAHA CORPORATION

YMU836 APPLICATION MANUAL
CATALOG No. LSI-6MU836A21
2015.9

IMPORTANT NOTICE

1. YAMAHA RESERVES THE RIGHT TO MAKE CHANGES TO ITS PRODUCTS AND TO THIS DOCUMENT WITHOUT NOTICE. THE INFORMATION CONTAINED IN THIS DOCUMENT HAS BEEN CAREFULLY CHECKED AND IS BELIEVED. HOWEVER, YAMAHA SHALL ASSUME NO RESPONSIBILITIES FOR INACCURACIES AND MAKE NO COMMITMENT TO UPDATE OR TO KEEP CURRENT THE INFORMATION CONTAINED IN THIS DOCUMENT.

2. THESE YAMAHA PRODUCTS ARE DESIGNED ONLY FOR COMMERCIAL AND NORMAL INDUSTRIAL APPLICATIONS, AND ARE NOT SUITABLE FOR OTHER USES, SUCH AS MEDICAL LIFE SUPPORT EQUIPMENT, NUCLEAR FACILITIES, CRITICAL CARE EQUIPMENT OR ANY OTHER APPLICATION THE FAILURE OF WHICH COULD LEAD TO DEATH, PERSONAL INJURY OR ENVIRONMENTAL OR PROPERTY DAMAGE. USE OF THE PRODUCTS IN ANY SUCH APPLICATION IS AT THE CUSTOMER'S OWN RISK AND EXPENSE.

3. YAMAHA SHALL ASSUME NO LIABILITY FOR INCIDENTAL, CONSEQUENTIAL OR SPECIAL DAMAGES OR INJURY THAT MAY RESULT FROM MISAPPLICATION OR IMPROPER USE OR OPERATION OF THE PRODUCT.

4. YAMAHA MAKES NO WARRANTY OR REPRESENTATION THAT THE PRODUCTS ARE SUBJECT TO INTELLECTUAL PROPERTY LICENSE FROM YAMAHA OR ANY THIRD PARTY, AND YAMAHA MAKES NO WARRANTY OR REPRESENTATION OF NON-INFRINGEMENT WITH RESPECT TO THE PRODUCTS. YAMAHA SPECIFICALLY EXCLUDES ANY LIABILITY TO THE CUSTOMER OR ANY THIRD PARTY ARISING FROM OR RELATED TO THE PRODUCTS INFRINGEMENT OF ANY THIRD PARTY'S INTELLECTUAL PROPERTY RIGHTS, INCLUDING THE PATENT, COPYRIGHT, TRADEMARK OR TRADE SECRET RIGHTS OF ANY THIRD PARTY.

5. EXAMPLES OF USE DESCRIBED HEREIN ARE MERELY TO INDICATE THE CHARACTERISTICS AND PERFORMANCE OF PRODUCTS. YAMAHA SHALL ASSUME NO RESPONSIBILITY FOR ANY INTELLECTUAL PROPERTY CLAIMES OR OTHER PROBLEMS THAT MAY RESULT FROM APPLICATIONS BASED ON THE EXAMPLES DESCRIBED HEREIN. YAMAHA MAKES NO WARRANTY WITH RESPECT TO THE PRODUCTS, EXPRESS OR IMPLIED, INCLUDING, BUT NOT LIMITED TO THE WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR USE AND TITLE.

6. YAMAHA MAKES EVERY EFFORT TO IMPROVE THE QUALITY AND RELIABILITY OF ITS PRODUCTS. HOWEVER, ALL SEMICONDUCTOR PRODUCTS FAIL WITH SOME PROBABILITY. THEREFORE, YAMAHA REQUIRES THAT SUFFICIENT CARE BE GIVEN TO ENSURING SAFE DESIGN IN CUSTOMER PRODUCTS SUCH AS REDUNDANT DESIGN, ANTI-CONFLAGRATION DESIGN, AND DESIGN FOR PREVENTING MALFUNCTION IN ORDER TO PREVENT ACCIDENTS RESULTING IN INJURY OR DEATH, FIRE OR OTHER SOCIAL DAMAGE FROM OCCURRING AS A RESULT OF PRODUCT FAILURE.

7. INFORMATION DESCRIBED IN THIS DOCUMENT: APPLICATION CIRCUITS AND ITS CONSTANTS AND CALCULATION FORMULAS, PROGRAMS AND CONTROL PROCEDURES ARE PROVIDED FOR THE PURPOSE OF EXPLAINING TYPICAL OPERATION AND USAGE. THEREFORE, PLEASE EVALUATE THE DESIGN SUFFICIENTLY AS WHOLE SYSTEM UNDER THE CONSIDERATION OF VARIOUS EXTERNAL OR ENVIRONMENTAL CONDITIONS AND DETERMINE THEIR APPLICATION AT THE CUSTOMER'S OWN RISK. YAMAHA SHALL ASSUME NO RESPONSIBILITY FOR CLAIMS, DAMAGES, COSTS AND EXPENSES CAUSED BY THE CUSTOMER OR ANY THIRD PARTY, OWING TO THE USE OF THE ABOVE INFORMATION.

PRECAUTIONS AND INSTRUCTIONS FOR SAFETY

	WARNING
Prohibited	Do not use the device under stresses beyond those listed in Absolute Maximum Ratings. Such stresses may become causes of breakdown, damages, or deterioration, causing explosion or ignition, and this may lead to fire or personal injury.
Prohibited	Do not mount the device reversely or improperly and also do not connect a supply voltage in wrong polarity. Otherwise, this may cause current and/or power-consumption to exceed the absolute maximum ratings, causing personal injury due to explosion or ignition as well as causing breakdown, damages, or deterioration. And, do not use the device again that has been improperly mounted and powered once.
Prohibited	Do not short between pins. In particular, when different power supply pins, such as between high-voltage and low-voltage pins, are shorted, smoke, fire, or explosion may take place.
Instructions	As to devices capable of generating sound from its speaker outputs, please design with safety of your products and system in mind, such as the consequences of unusual speaker output due to a malfunction or failure. A speaker dissipates heat in a voice-coil by air flow accompanying vibration of a diaphragm. When a DC signal (several Hz or less) is input due to device failure, heat dissipation characteristics degrade rapidly, thereby leading to voice-coil burnout, smoking or ignition of the speaker even if it is used within the rated input value.

	CAUTION
Prohibited	Do not use Yamaha products in close proximity to burning materials, combustible substances, or inflammable materials, in order to prevent the spread of the fire caused by Yamaha products, and to prevent the smoke or fire of Yamaha products due to peripheral components.
Instructions	Generally, semiconductor products may malfunction and break down due to aging, degradation, etc. It is the responsibility of the designer to take actions such as safety design of products and the entire system and also fail-safe design according to applications, so as not to cause property damage and/or bodily injury due to malfunction and/or failure of semiconductor products.
Instructions	The built-in DSP may output the maximum amplitude waveform suddenly due to malfunction from disturbances etc. and this may cause damage to headphones, external amplifiers, and human body (the ear). Please pay attention to safety measures for device malfunction and failure both in product and system design.
Instructions	As semiconductor devices are not nonflammable, overcurrent or failure may cause smoke or fire. Therefore, products should be designed with safety in mind such as using overcurrent protection circuits to control the amount of current during operation and to shut off on failure.
Instructions	Products should be designed with fail safe in mind in case of malfunction of the built-in protection circuits. Note that the built-in protection circuits such as overcurrent protection circuit and high-temperature protection circuit do not always protect the internal circuits. In some cases, depending on usage or situations, such protection circuit may not work properly or the device itself may break down before the protection circuit kicks in.
Instructions	Use a robust power supply. The use of an unrobust power supply may lead to malfunctions of the protection circuit, causing device breakdown, personal injury due to explosion, or smoke or fire.
Instructions	Product's housing should be designed with the considerations of short-circuiting between pins of the mounted device due to foreign conductive substances (such as metal pins etc.). Moreover, the housing should be designed with spatter prevention etc. due to explosion or burning. Otherwise, the spattered substance may cause bodily injury.
Instructions	The device may be heated to a high temperature due to internal heat generation during operation. Therefore, please take care not to touch an operating device directly.
Instructions	Electrostatic discharges can damage and destroy semiconductor devices. Pay close attention to static build-up when handling devices.
Instructions	The product of the WLCSP package should be used under light-shielded conditions. Since the WLCSP package has a structure that a silicon wafer is exposed, if light (such as sunlight) hits the wafer, the device may malfunction (leak current increase etc.) due to electric charge internally generated by the photoelectric effect.

v04

Table of Contents

1 Symbols, Marks, and Notations

Icons used in this document

Indicates prohibited matters.

Indicates precautions to be taken into consideration.

Indicates noteworthy restrictions and pitfalls in application.

Indicates supplementary information and applications hints.

Numbers

Numbers are expressed in the form: <size> <base_format> <number>. In this form, <size>, size in bits, and <base_format> elements are optional. Single bits, binary numbers of 1-bit size, are expressed in another form that is described later in this section.

Example: *The value of* ***15*** *(in decimal) expressed in different bases:*

- *Binary:* ***8'b 0000_1111***
- *Decimal:* ***15*** *(of unspecified size and in the default base of 10)*
- *Hexadecimal:* ***8'h0F***

Bit/Digit Order
The most significant bit or digit appears first in <number>, followed by progressively less significant bits, and the least significant bit or digit at the end.

Example: 8’b1000_1110
MSB LSB

Binary value is thus converted to its corresponding value using

$(2^n \times Dn) + \cdots + (2^1 \times D1) + (2^0 \times D0)$

Example:

If REG_A register is described as:

D7	D6	D5	D4	D3	D2	D1	D0
B_ADR							

and when D7 through D0 has the value of 8'b 0001_0101,
B_ADR value in decimal is 21. $(21 = 2^4 + 2^2 + 2^0)$

Register and Memory Addresses

Addresses are preceded by the pound mark "#" when represented in decimal. (Example: #0, #1 ...)
Addresses are preceded by "0x" when represented in hexadecimal. (Example: 0x00)

Single Bit Notations

Logic signal level on input and output pins is represented as "L" or "H".

Otherwise, it is represented as "0" or "1".

Term Definition

Power Save

Digital Block: A state where digital blocks are powered but clocks fed to them are stopped.

Analog Block: A state where individual power saving register is set to "1".

See *6.2 Device Startups and Power Management* for details.

Other Symbols and Terms

Sample Rates

The system sample rate used for internal processing is shown as fs_{SY}.
The rate used for digital audio input samples is shown as fs_{DA}.

Accessibility During Power Save

- Writing
  "Access During Power Save State" in each register description says *"Allowed"* if writing is valid, *"Not allowed"* if not, when the digital core is in power-saving state.
- Reading
  "Access During Power Sava State" in each register description says *"Allowed"* if the read access returns valid data, *"Not allowed"* if not, when the digital core is in power-saving state.

2 Overview

YMU836 (AVP-2) is a voice and audio codec SoC for automotive applications.

- Yamaha AudioEngine™ HD, programmable high-quality audio effects using 32-bit floating point DSP.
- Hands-free sound processor for conversations in noisy places typical in automotive applications, suppressing noise and keeping voice intelligible. Works on transmit- and receive-path speeches and for voice recognition.
- Host controller and other interfaces supporting connections to various automotive audio systems. Microphones (analog 4 ch. / digital 4 ch.), line level outputs (4 ch.), 2 digital interface ports (I^2S stereo input/output)
- On-chip MPU (Micro Processor Unit) allowing for standalone operations without external hosts

Features

Open Core DSP

- Programmable sound effects
- 294MIPS, 176kB RAM

Speech

- Dual microphone noise suppressor
- Dual mic beam-forming directionality control
- Echo canceller with long echo tail support
- Proprietary voice intelligibility improver

Audio

- Four 64-oversampling 24−bit DEM DACs
- Four 128−oversampling 24-bit ΔΣADCs
- Multi-band DRC, PEQ, AGC
- AEQ to fine-tune total acoustic paths
- Harmonic enhancer processing

Others

- Pb-free 64-pin QFN (YMU836-QZ)
  9.00 mm (W) × 9.00 mm (D) × 0.90 mm (H)
- Temp. −40°C to +85°C

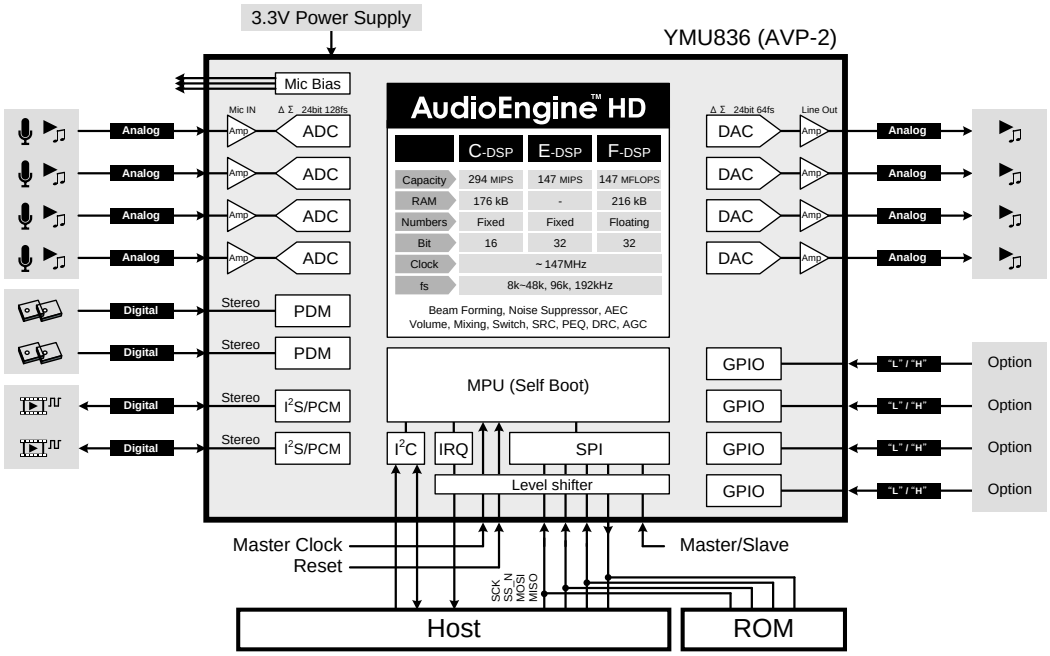


Figure 2-1. YMU836 blocks.

2.1 Features

2.1.1 DSP Functions

VOICE Tx
HFK5.1 Option (Hands Free Kit 5.1) Hand Set / Hands Free / Voice Recognition 8kHz / 16kHz / 24kHz Super Wide Band - BF 2-Mic Beam Forming with Voice tracking - NS 1/2-Mic Noise Suppressor - AEC Acoustic Echo Canceller - FFP Far Field Pick up - PEQ 5-Band PEQ - DRC Single Band DRC - AGC Automatic Gain Control
DOA360 Option (Direction of Arrival)
Voice Trigger Option

VOICE Rx
HFK5.1 Option (Hands Free Kit 5.1) Hand Set / Hands Free 8kHz / 16kHz / 24kHz Super Wide Band - NS Noise Suppressor - BVE Bright Voice Engine - PEQ 5-Band PEQ - HPF High Pass Filter - DRC Single Band DRC - AGC Automatic Gain Control

REC
Rec Enhancer (EQ + AGC / DRC)
VRK5.0 Option (Voice Recognition 5.0) 2-MIC Directional Recording 1-MIC Omni Recording

PLAY
SRC 8k,16k,24k,32k,44.1k,48k,96k,192kHz → 48kHz
Line Out Compensation - AEQ Acoustic total-linear EQ - SE Stereo Enhancer - HXT Harmonics enhancer Extended - PEQ 3-Band PEQ - DRC 3-Band + Single Band Multi Point DRC
Audio Enhancer B 22Surround + HXT + EQ + Multi Band DRC
Audio Enhancer C AEQ + 22Surround
Audio Enhancer F AEQ + 252Surround + EQ + Multi Band DRC
Super Hi-Fi Option
Karaoke Option
Hearing Aid Option

Others	
Open Core DSP	294MIPS, 176kB RAM, 16bit Fixed Point DSP, fs = 8 kHz to 48 kHz (Direct: 96 kHz/192 kHz)

2.1.2 General Functions

DSP	
Main Core	Quad Core – B/C/E/F DSP E-DSP : 147 MIPS : 32bit Fixed Point : Clock, 73 MHz F-DSP : 147 MFLOPS : 32bit Floating Point : Clock, up to 147.456 MHz
Open Core	294MIPS,176kB RAM : 16bit Fixed Point : Fs, 8 kHz to 48 kHz (Direct: 96 kHz/192 kHz) : Clock, up to 147.456 MHz

Digital Basic Functions	
Digital Volume	–95 to +18dB /1dB step
Digital Mixer	Multi-Channel Flexible
Mono Mixing	L+R, (L+R)/2, …
L/R Switch	L/R, R/L, L/L, R/R
Loop Back	Flexible

PEQ - Parametric Equalizer	
Band	3-Band/5-Band/3+3/…
PEQ	Peaking Equalizer
BPF	Band Pass Filter
BEF	Band Elimination Filter
HSF	High Shelving Filter
LSF	Low shelving Filter
HPF	High Pass Filter
LPF	Low Pass Filter

Audio Data Format	
Port	1/2 – Stereo x 2 Port
Format	I^2S, PCM
Data Length	16/20/24 bit
LRCK Length	8/16/24/32/48/ 64/96/128/192/256/512 bit
Sampling	8k/11.025k/12k/16k/22.05k/ 24k/32k/44.1k/48kHz/Auto
Direction	Master / Slave
Hi-z Timing	Normal / Invert
Frame mode	Short / Long
Receive	Rise / Fall

Digital MIC Format	
Channel	Stereo x 2 Port
Sampling	32/64/128fs
Wait	0/1/10/20 ms
Load Time	PDMCK Edge
Before	27/54/81/108 ns
After	27/54/81 ns
Data Delay	L/R Fine Tuning

Support	
Driver	Linux / Generic
Tuning Tool	Audio Engine Studio
Tuning Service	by Sound Engineers by Voice Call Engineers

3 Block Diagram

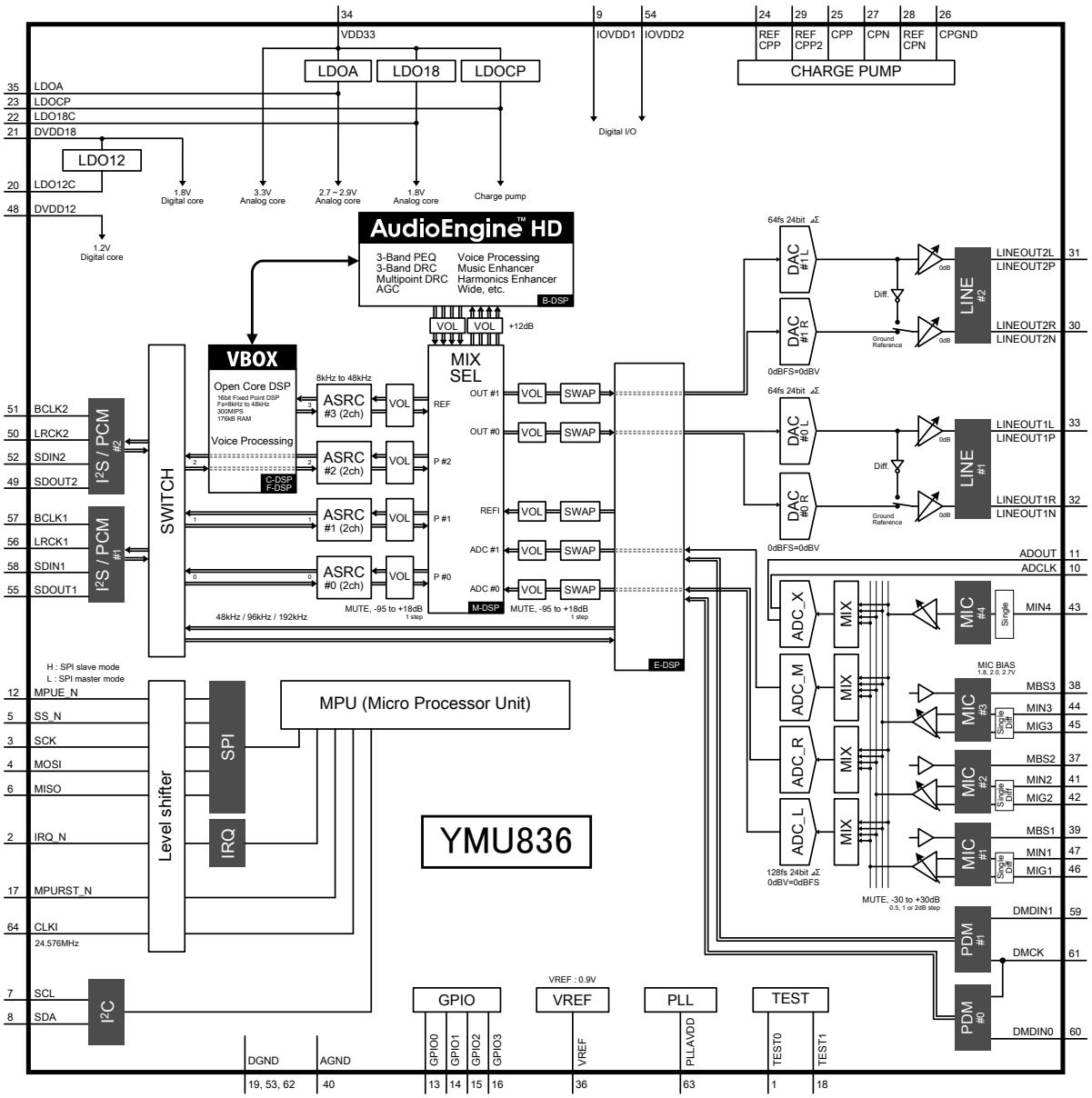


Figure 3-1. Package pinout.

4 Pin Assignments

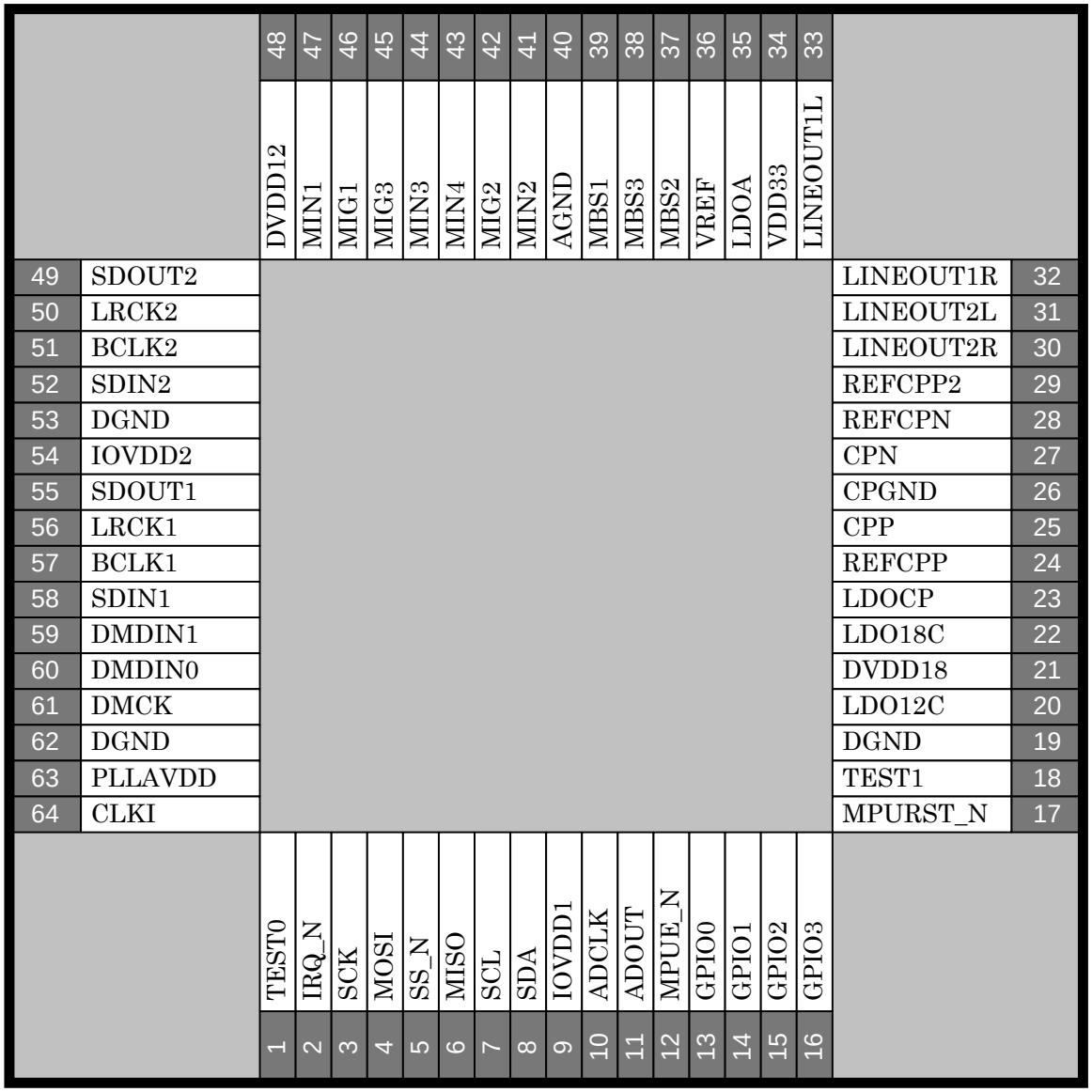


Figure 4-1. 64-pin QFN (Top View).

5 Pin Descriptions

5.1 Pin Summary

Table 5.1. Pin Summary

No.	Pin name	I/O	Power supply	Function
1	TEST0	I	IOVDD1	Test pin#0 (Tie to DGND)
2	IRQ_N	Ot	IOVDD1	SPI master mode (MPUE_N = “L”): Connect this pin to DGND. SPI slave mode (MPUE_N = “H”): Interrupt request output Pull up this pin with a resistor ranging from 10 kΩ to 200 kΩ. There is a tradeoff between consumption power and capacitive load. Connect the pin to DGND when not used.
3	SCK	I_{SH}/O	IOVDD1	SPI clock
4	MOSI	I_{SH}/O	IOVDD1	SPI data input
5	SS_N	I_{SH}/O	IOVDD1	SPI slave selection
6	MISO	I_{SH}/Ot	IOVDD1	SPI data output Using a resistor ranging from 100 kΩ to 220 kΩ is recommended for the pull-up/pull-down.
7	SCL	I_{SH}	IOVDD1	I^2C slave interface: clock input
8	SDA	I_{SH}/Od	IOVDD1	I^2C slave interface: data input and output
9	IOVDD1	P	–	IO supply (2.80 V to 3.60 V) (except for Digital audio#2)
10	ADCLK	I_{SH}	IOVDD1	ADC_X clock input Connect this pin to DMCK.
11	ADOUT	O	IOVDD1	ADC_X data output Connect this pin to DMDIN0 or DMDIN1.
12	MPUE_N	I_{SH}	IOVDD1	On-chip MPU Enable/Disable, SPI interface Master/Slave select "L": Enables on-chip MPU and selects SPI master mode. "H": Disables on-chip MPU and selects SPI slave mode.
13	GPIO0	I_{SH}/O	IOVDD1	GPIO port #0
14	GPIO1	I_{SH}/O	IOVDD1	GPIO port #1
15	GPIO2	I_{SH}/O	IOVDD1	GPIO port #2
16	GPIO3	I_{SH}/O	IOVDD1	GPIO port #3
17	MPURST_N/ SPIMODE	I_{SH}	IOVDD1	SPI master mode (MPUE_N = “L”): Resetting on-chip MPU ("L": Reset) SPI slave mode (MPUE_N = “H”): Selecting SPI mode ("L": Modes 0, 3 / "H": Modes 1, 2)
18	TEST1	I	IOVDD1	Test pin#1 (Connect to DGND pin.) Used for writing to ROM (Driving this input "H" puts SPI pin into high-impedance state.
19	DGND	G	–	Digital ground
20	LDO12C	AO	DVDD18	LDO12 output (Decouple to DGND through a 2.2 µF capacitor)
21	DVDD18	P	–	Digital power supply Connect this pin to LDO18C.
22	LDO18C	AO	VDD33	LDO18 output (Decouple to DGND through a 2.2 µF capacitor)

No.	Pin name	I/O	Power supply	Function
23	LDOCP	AO	VDD33	LDOCP output (Decouple to CPGND through a 47 µF capacitor)
24	REFCPP	AO	LDOCP	Charge pump output (Pos.)
25	CPP	AO	LDOCP	Charge pump capacitor connection (Pos.)
26	CPGND	AG	–	Charge pump ground
27	CPN	AO	LDOCP	Charge pump capacitor connection (Neg.)
28	REFCPN	AO	LDOCP	Charge pump output (Neg.)
29	REFCPP2	AO	LDOCP	Charge pump output (Pos. #2) Connect to REFCPP pin.
30	LINEOUT2R/ LINEOUT2N	AO	LDOCP	Line output #2 (R channel / differential minus)
31	LINEOUT2L/ LINEOUT2P	AO	LDOCP	Line output #2 (L channel / differential plus)
32	LINEOUT1R/ LINEOUT1N	AO	LDOCP	Line output #1 (R channel / differential minus)
33	LINEOUT1L/ LINEOUT1P	AO	LDOCP	Line output #1 (L channel / differential plus)
34	VDD33	P	–	Power supply (2.80 V to 3.60 V)
35	LDOA	AO	VDD33	LDOA output (Decouple to AGND through a 2.2 µF capacitor)
36	VREF	AO	LDOA	Analog reference voltage (Decouple to AGND through a 1 µF capacitor)
37	MBS2	AO	LDOA	Microphone bias output #2
38	MBS3	AO	LDOA	Microphone bias output #3
39	MBS1	AO	LDOA	Microphone bias output #1
40	AGND	AG	–	Analog ground
41	MIN2	AI	LDO18	Microphone input #2
42	MIG2	AI	LDO18	Microphone input #2 (for differential signal inputs)
43	MIN4	AI	LDO18	Microphone input #4
44	MIN3	AI	LDO18	Microphone input #3
45	MIG3	AI	LDO18	Microphone input #3 (for differential signal inputs)
46	MIG1	AI	LDO18	Microphone input #1 (for differential signal inputs)
47	MIN1	AI	LDO18	Microphone input #1
48	DVDD12	P	–	Digital power supply Connect to LDO12C pin.
49	SDOUT2	Ot	IOVDD2	Digital audio #2: data output
50	LRCK2	I/O	IOVDD2	Digital audio #2: LR clock
51	BCLK2	I/O	IOVDD2	Digital audio #2: bit clock
52	SDIN2	I	IOVDD2	Digital audio #2: data input
53	DGND	G	–	Digital ground
54	IOVDD2	P	–	Digital audio #2: IO power supply (1.65 V to 1.95 V / 2.80 V to 3.60 V)
55	SDOUT1	Ot	IOVDD1	Digital audio #1: data output
56	LRCK1	I/O	IOVDD1	Digital audio #1: LR clock
57	BCLK1	I/O	IOVDD1	Digital audio #1: bit clock
58	SDIN1	I	IOVDD1	Digital audio #1: data input

No.	Pin name	I/O	Power supply	Function
59	DMDIN1	I/O	IOVDD1	Digital microphone: data input #1 / AD data input (Connect to ADOUT pin)
60	DMDIN0	I/O	IOVDD1	Digital microphone: data input #0 / AD data input (Connect to ADOUT pin)
61	DMCK	I/O	IOVDD1	Digital microphone: clock output / AD clock output (Connect to ADCLK pin)
62	DGND	G	–	Digital ground
63	PLLAVDD	P	–	PLL power supply (Connect to LDO12C pin)
64	CLKI	I_{SH}	IOVDD1	Clock input

Table 5.2. I/O Symbols

Pin type	
I	Digital input
O	Digital output
I/O	Digital input and output
I_{SH}	Digital input (Schmitt trigger input)
I_{SH}/O	Digital input (Schmitt trigger input) and digital output
I_{SH}/Ot	Digital input (Schmitt trigger input) and tri-state output
I_{SH}/Od	Digital input (Schmitt trigger input) and digital output (open-drain)
Ot	Tri-state output
AI	Analog input
AO	Analog output
P	Power supply
G	Ground
AG	Analog Ground

All supply pins are isolated from each other inside the device. All ground connections are connected to the substrate inside the device.

5.2 Device Pin States

5.2.1 Device Pin States During and On Exiting Power-on Resets

Floating input pins must not be left at nor applied a voltage in the middle of power rails.

Table 5.3. Device Pin States During and On Exiting Power-on Resets (Digital)

(Digital) Pin	Pin state on reset
SCL, SDA, MPURST_N, MPUE_N, GPIO[0/1/2/3], ADCLK, SDIN[1/2], LRCK[1/2], BCLK[1/2], CLKI, DMDIN[0/1], DMCK	High-impedance state (input)
SS_N, SCK	MPUE_N = "L": High-impedance state during Power-on Reset, Low-impedance state (output) on exiting resets MPUE_N = "H": High-impedance state (input)
MOSI	MPUE_N ="L": High-impedance state during Power-on Reset, Low-impedance state (output) on exiting resets MPUE_N ="H": High-impedance state
MISO	MPUE_N ="L": High-impedance state (input) MPUE_N ="H": High-impedance state (output)
IRQ_N	High-impedance state (output)
ADOUT	High-impedance state during Power-on Reset, Low-impedance state (output) on exiting resets
SDOUT[1/2]	High-impedance state Setting SDO*_DDR registers to "1" changes port data direction to output.
TEST[0/1]	High-impedance state (input) Tie this pin to "L" (DGND).

Table 5.4. Device Pin States During or On Exiting Power-on Resets (Analog)

(Analog) Pin	Pin state on reset	
	During and on exiting Power-On Resets	With active analog block (See Note 1.)
CPP	D (0 V)	P
CPN		
LDOA	Z (0 V)	D (LDOA)
LDO18C	D (LDO18)	D (LDO18)
LDO12C	Z (0 V)	D (LDO12)
LINEOUT1L / LINEOUT1P	D (0 V)	D (0 V)
LINEOUT1R / LINEOUT1N		
LINEOUT2L / LINEOUT2P		
LINEOUT2R / LINEOUT2N		
MBS1	F/D (0 V), MBS1_DISCH = 0 / 1	D (MBS1)
MBS2	F/D (0 V), MBS2_DISCH = 0 / 1	D (MBS2)
MBS3	F/D (0 V), MBS3_DISCH = 0 / 1	D (MBS3)
MIG[1/2/3]	F	Z (VREF)
MIN[1/2/3/4]		
REFCPN	D (0 V)	D (REFCPN)
REFCPP	Z (0 V)	D (REFCPP)
REFCPP2	Z (0 V)	D (REFCPP2)
VREF	D (0 V)	Z (VREF)

F: High impedance state (floating)
Z: High impedance state holding the voltage in parentheses
D: Low impedance state holding the voltage in parentheses
P: Pulsed output (low-impedance)

Note 1: When at least one of AP_* registers (ANA_REG#2–#7) is set to "0".

The device is assumed to be working in the following conditions:
No sound is playing when any analog block is in use.
Each of REFCPP, REFCPP2, CPP, CPN, REFCPN, MBS1/2/3, LDOA, LDO12C, and LDO18C pins has the default value capacitor as described in this document.

5.2.2 Handling of Unused Pins

◆ **Digital Pins:**

Input Pins

Table 5.5. Digital Input Pins

Pin name	When not in use:
SCL	Tie to "L" level.
Other pins	Tie to "L" or "H" level. Leave them open when the input mask function is enabled. For details, see *Pins With Input Mask Function* shown below.

Output Pins

Table 5.6. Digital Output Pins

Pin name	When not in use:
-	Leave this pin open.

Input and Output Pins

Table 5.7. Digital Input and Output Pins

Pin name	When not in use:
SDA	Tie to "L" level.
Other pins	Tie to "L" or "H" level. Leave them open when the input mask function is enabled. For details, see *Pins With Input Mask Function* shown below.

Pins With Input Mask Function

Table 5.8. Digital Pins With Input Mask Function

Pin name	I/O	Input mask control register
BCLK1	I/O	BCLK1_MSK
BCLK2	I/O	BCLK2_MSK
LRCK1	I/O	LRCK1_MSK
LRCK2	I/O	LRCK2_MSK
SDIN1	I	SDIN1_MSK
SDIN2	I	SDIN2_MSK
DMCK	I/O	PA0_MSK
DMDIN0	I/O	PA1_MSK
DMDIN1	I/O	PA2_MSK
GPIO0	I_{SH}/O	GP0_MSK
GPIO1	I_{SH}/O	GP1_MSK
GPIO2	I_{SH}/O	GP2_MSK
GPIO3	I_{SH}/O	GP3_MSK
ADCLK	I_{SH}	DP_ADCLK

◆ Analog Pins

Table 5.9. Analog Pins

Pin name	When not in use:
LINEOUT1L, LINEOUT1R, LINEOUT2L, LINEOUT2R, MIN1, MIG1, MIN2, MIG2, MIN3, MIG3, MIN4, MBS1, MBS2, MBS3	Leave this pin open.

All supply pins must be powered whether they are used or not.

6 Device Operations

6.1 Host Controller Interface

YMU836's host controller interface supports two different types of interfaces:

- I^2C (slave)
- SPI (master / slave)

I^2C, however, is available only in SPI master mode (on-chip MPU being activated).

SPI

SPI (Serial Peripheral Interface) is a serial communication interface specification developed by Motorola and has become a de-facto standard.

I^2C

I^2C is a serial interface bus designed by NXP Semiconductors (former Philips Semiconductors).

6.1.1 SPI

YMU836 supports SPI modes 0 through 3.
Use SPIMODE pin to select a mode (in SPI slave mode).
MODE 0 is selected when in SPI master mode.

MODE 0, MODE 3 (Rising edge Trigger): SPIMODE pin = "L"

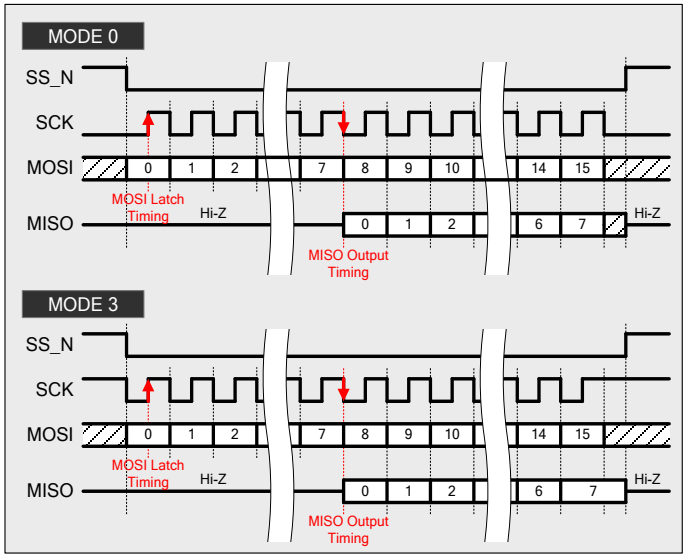


Figure 6-1. SPI modes 0, 3.

MODE 1, MODE 2 (Falling edge Trigger): SPIMODE-pin = "H"

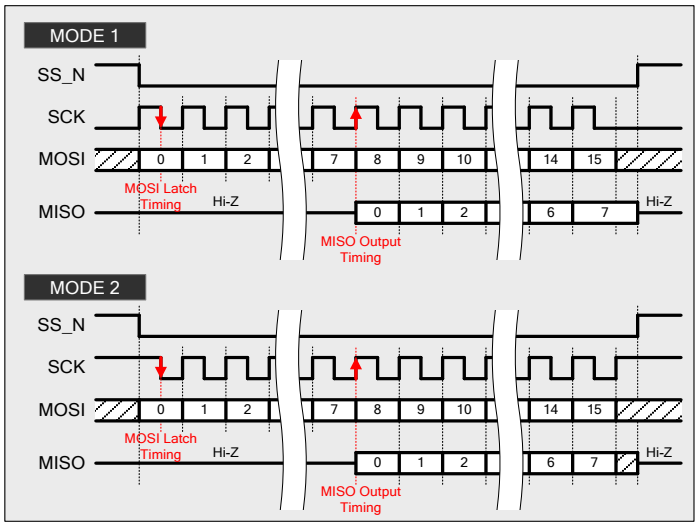


Figure 6-2. SPI modes 1, 2.

6.1.1.1 SPI Signals and Pins

Figures below show basic master-slave configurations.

SPI Master Mode (MPUE_N = "L")

YMU836 acts as a master device, and Flash Memory as a slave.

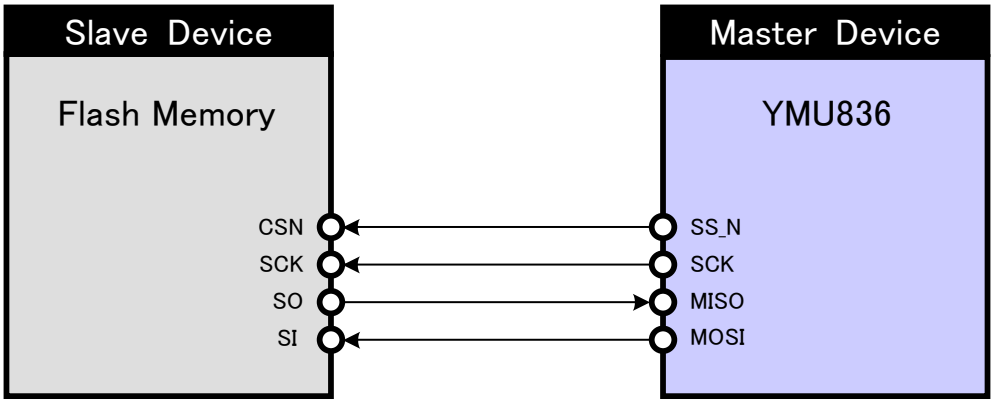


Figure 6-3. Master-Slave control signals.

Each pin used for the interface works as follows.

Table 6.1. Pin Functions (With External Memory Connected)

Pin Name	YMU836 I/O	Description
SS_N	O	Chip select to select a slave chip ("L" active)
SCK	O	Clock output
MISO	I	Data input
MOSI	O	Data output

MISO pin must be externally pulled up or down.

SPI Slave Mode (MPUE_N = "H")

The host controller acting as the master device controls the slave YMU836.

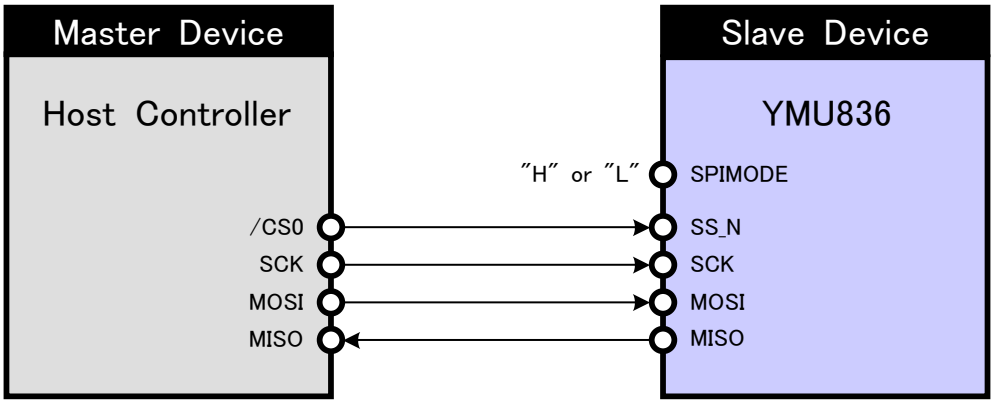


Figure 6-4. Master–Slave control signals.

Each pin used for the interface works as follows.

Table 6.2. Host Controller Interface Pins

Pin Name	YMU836 I/O	Description
SPIMODE	I	SPI mode select
SS_N	I	Chip select to select the slave chip (Active "L")
SCK	I	Clock input
MOSI	I	Data input
MISO	Ot	Data output

MISO pin must be externally pulled up or down.

6.1.1.2 Reading and Writing Registers

Registers can be read and written one byte at a time or multiple bytes at a time in burst.

- Set Reading and Writing : W/R bit (MSB in the command byte)
  - "L": Writing
  - "H": Reading
- Set single access and burst accesses : BA bit (LSB in the command byte)
  - "L": single read/write
  - "H": burst reads/writes

6.1.1.3 Single Byte Writes

Single byte of data, one at a time, can be written with sending a command and data pair (one byte plus one byte, 16 bits).

The command byte comes before the data byte to be written.
The host controller sends these bytes in this order while *SS_N* is held at "L". Raising *SS_N* ("H") after each write is not needed.
MISO enters the high impedance state during write accesses.

A single byte write sequence and timing in SPI MODE 0 is shown below.

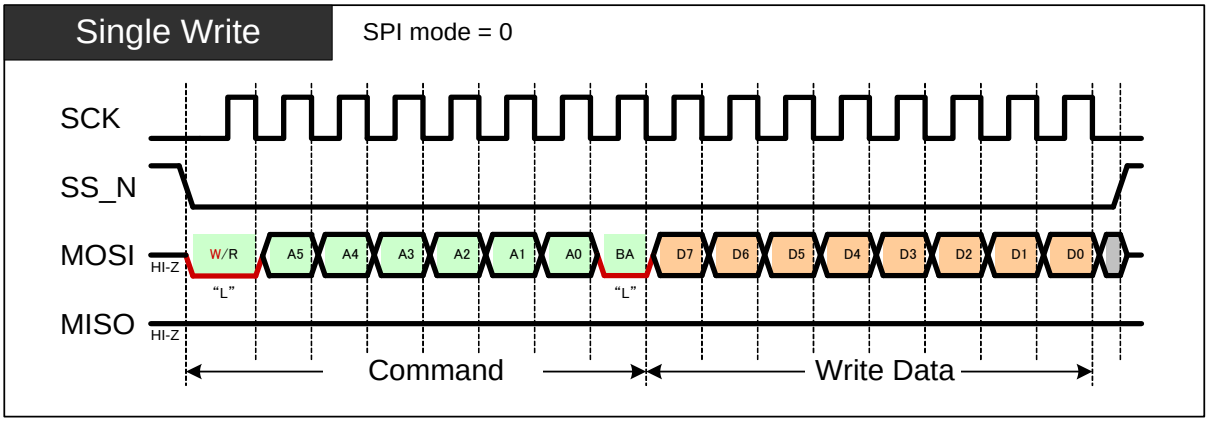


Figure 6-5. Single write timing chart.

Each bit timing in the chart means as follows.

Table 6.3. Bit Timing Description

Bit Timing	Description
W/R	Write or read (MSB) "L" for write access "H" for read access
A5–A0	Register address *Interface Register* address to be read or written
BA	Burst or single (LSB) "L" for single byte write/read "H" for burst writes/reads
D7–D0	Byte data to be written in MSB-first order

Write accesses must be in exactly two-byte-long (16 bit) sequences. Raising *SS_N* high earlier, like at 14 bit time, may lead to an unintended access and control.

***MISO* goes into the high impedance state during write accesses.**

6.1.1.4 Burst Writes

Multiple bytes of data can be written following a single burst write command byte.

- The command byte comes first
  - The top most bit in the command byte (BA) is "H" for burst writes
  - Other bits in the command byte is the same as single byte writes
  - Each additional data increments write data pointer
- Data bytes follows
- Raising *SS_N* "H" ends burst writes

A burst write sequence and timing is shown below.

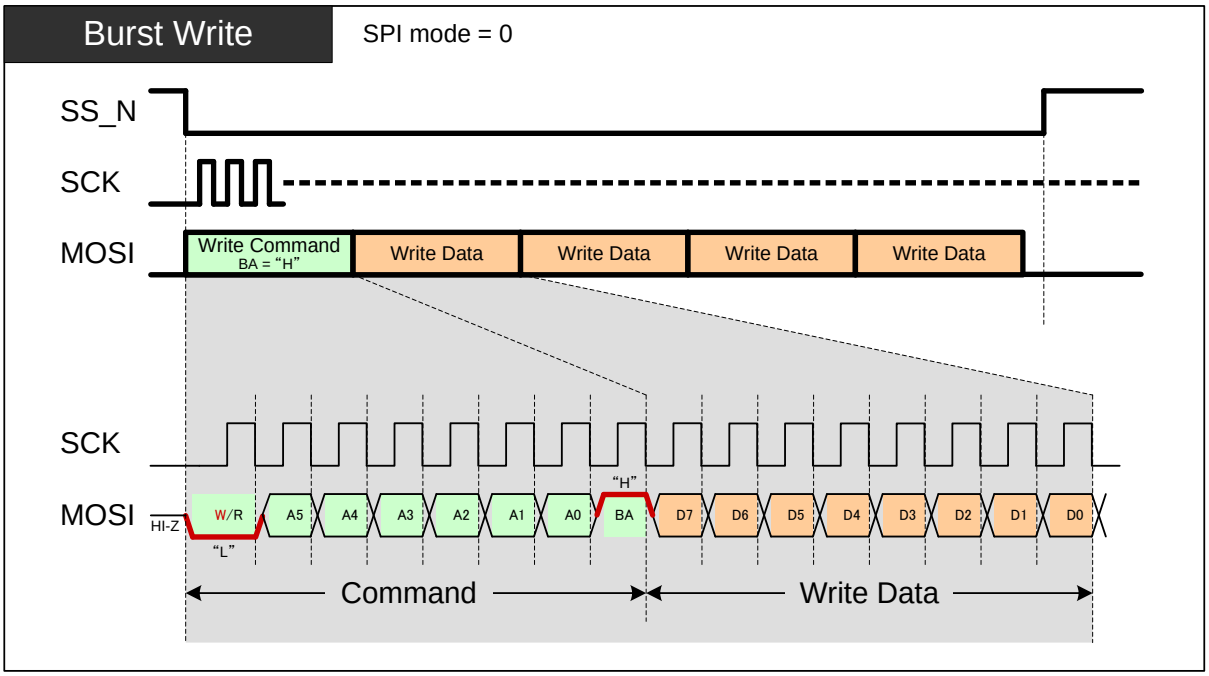


Figure 6-6. Burst write timing chart.

See *6.1.1.3 Single Byte Writes* for command or data bit information.

Each burst write data must be exactly one-byte-long (8 bit). Raising *SS_N* high earlier, like at 6 bit time, may lead to an unintended access and control.

***MISO* goes into the high impedance state during write accesses.**

6.1.1.5 Single Byte Reads

Single byte of data, one at a time, can be read in a 2 byte or 16 bit access frame.

The host controller holds *SS_N* at "L" while sending a single byte read command bytes and reading a data byte. Raising *SS_N* ("H") after each read is not needed. You can make as many single byte reads as you like as long as *SS_N* is held low.

A single byte read sequence and timing in SPI MODE 0 is shown below.

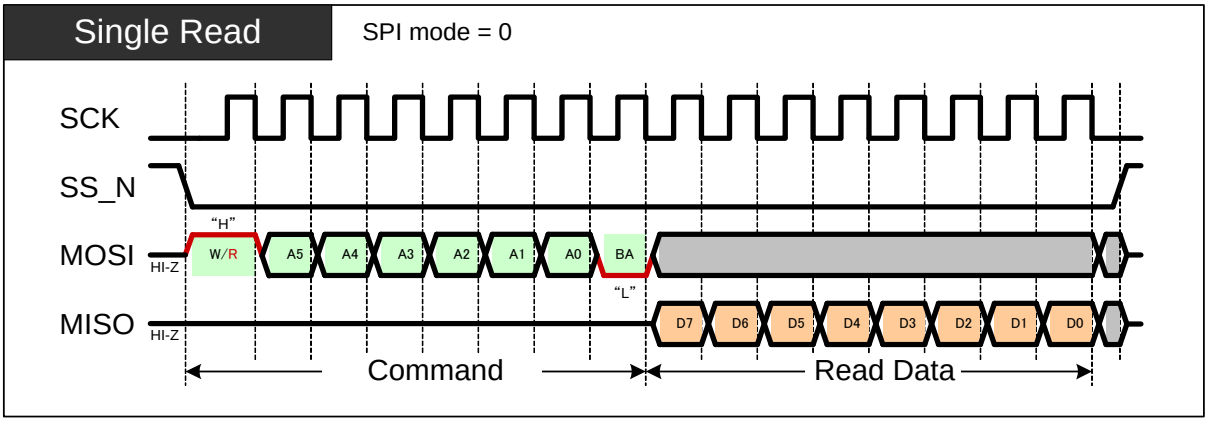


Figure 6-7. Single read timing chart.

Bit timings in the command and data mean as follows.

Table 6.4. Bit Timing Description

Bit Timing	Description
W/R	Write or read (MSB) "L" for write access "H" for read access
A5–A0	Register address *Interface Register* address to be read or written
BA	Burst or single (LSB) "L" for single byte write/read "H" for burst writes/reads
D7–D0	Byte data read data at the [A5:A0] address in MSB-first order

Read accesses must be in exact two-byte-long (16 bit) sequences. Raising *SS_N* high earlier, like at 14 bit time, may lead to an unintended access and consequence.

***MISO* goes into the high impedance state during *Command* byte transfers.**

***MOSI* must be driven to a valid logic level during *Data* byte transfers.**

6.1.1.6 Burst Reads

Multiple bytes of data can be read following a single burst read command byte.

- The command byte comes first
  - The top most bit in the command byte (BA) is "H" for burst reads
  - Other bits in the command byte is the same as single byte reads
  - Each additional data increments read data pointer
- Data bytes follows
- Raising *SS_N* "H" ends burst writes

A burst read sequence and timing in SPI MODE 0 is shown below.

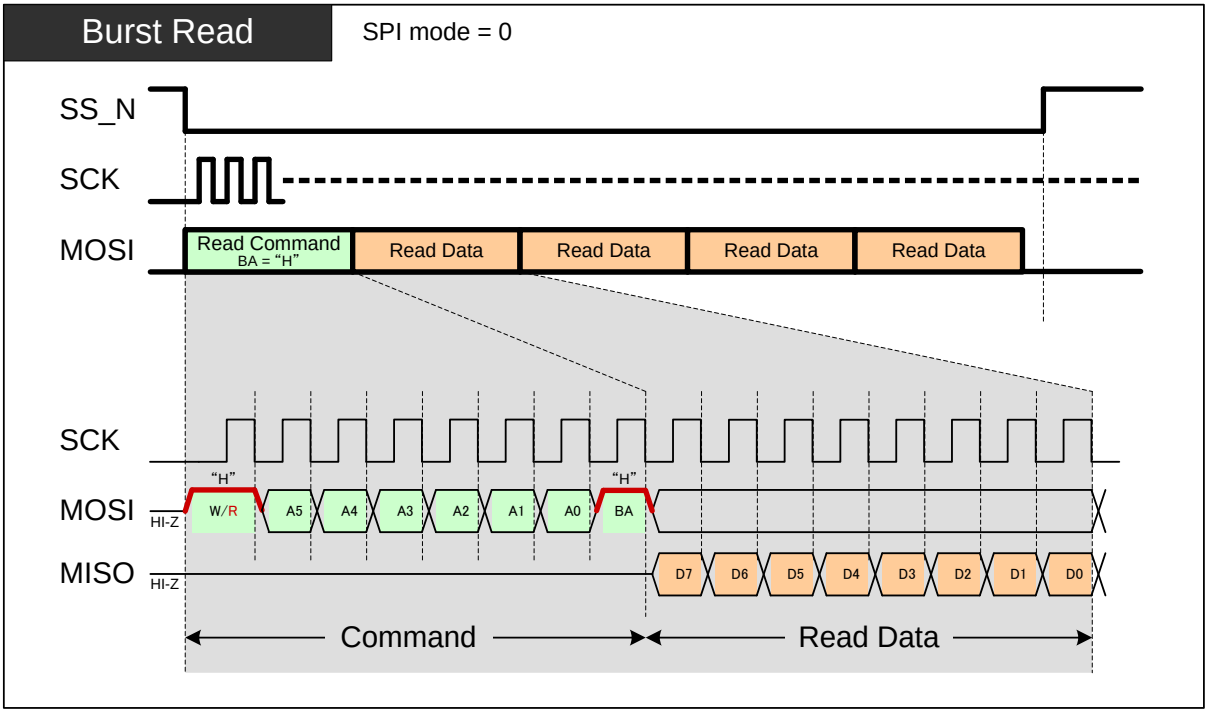


Figure 6-8. Burst read timing chart.

See *6.1.1.5 Single Byte Reads* for command or data bit information.

Use exactly one-byte-long (8 bit) frames to read data. Raising *SS_N* high earlier, like at 6 bit time, may lead to an unintended access and consequence.

***MISO* goes into the high impedance state during *Command* byte transfers.**

***MOSI* must be driven to a valid logic level during *Data* byte transfers.**

6.1.2 I²C

I²C uses two lines, SCL and SDA.

YMU836's I²C bus connected to on-chip MPUs is available only in SPI master mode.

6.1.2.1 Pin Function

The figure below shows a basic master-slave configuration. A device acting as an master device controls the slave YMU836.

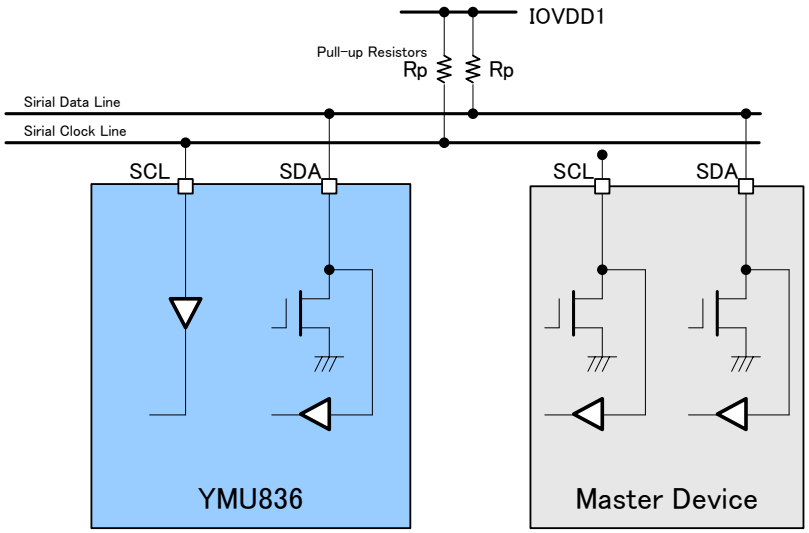


Figure 6-9. Master-Slave connections.

The table below shows pin functions.

Pin Name	I/O	Description
SCL	I	Clock input
SDA	I/O	Data input and output

6.1.2.2 I²C Slave Address

The slave address assigned to the device is "7'h3A".

Hex	A6	A5	A4	A3	A2	A1	A0
7'h3A	0	1	1	1	0	1	0

6.2 Device Startups and Power Management

6.2.1 LDO

YMU836 provides the following four kinds of LDOs (Low Dropout regulators).

Name	Power Source	Description
LDO18	VDD33	1.8 V digital core power supply (DVDD18) 1.8 V analog circuitry power supply
LDOCP	VDD33	1.8 V charge-pump power supply
LDOA	VDD33	2.7 V to 2.9 V analog circuitry power supply (register controlled supply voltage)
LDO12	DVDD18	1.2 V digital core power supply (DVDD12) PLL power supply (PLLAVDD)

・DVDD18 must be supplied from LDO18 output (LDO18C pin).

・DVDD12 and PLLAVDD must be supplied from LDO12 output (LDO12C pin).

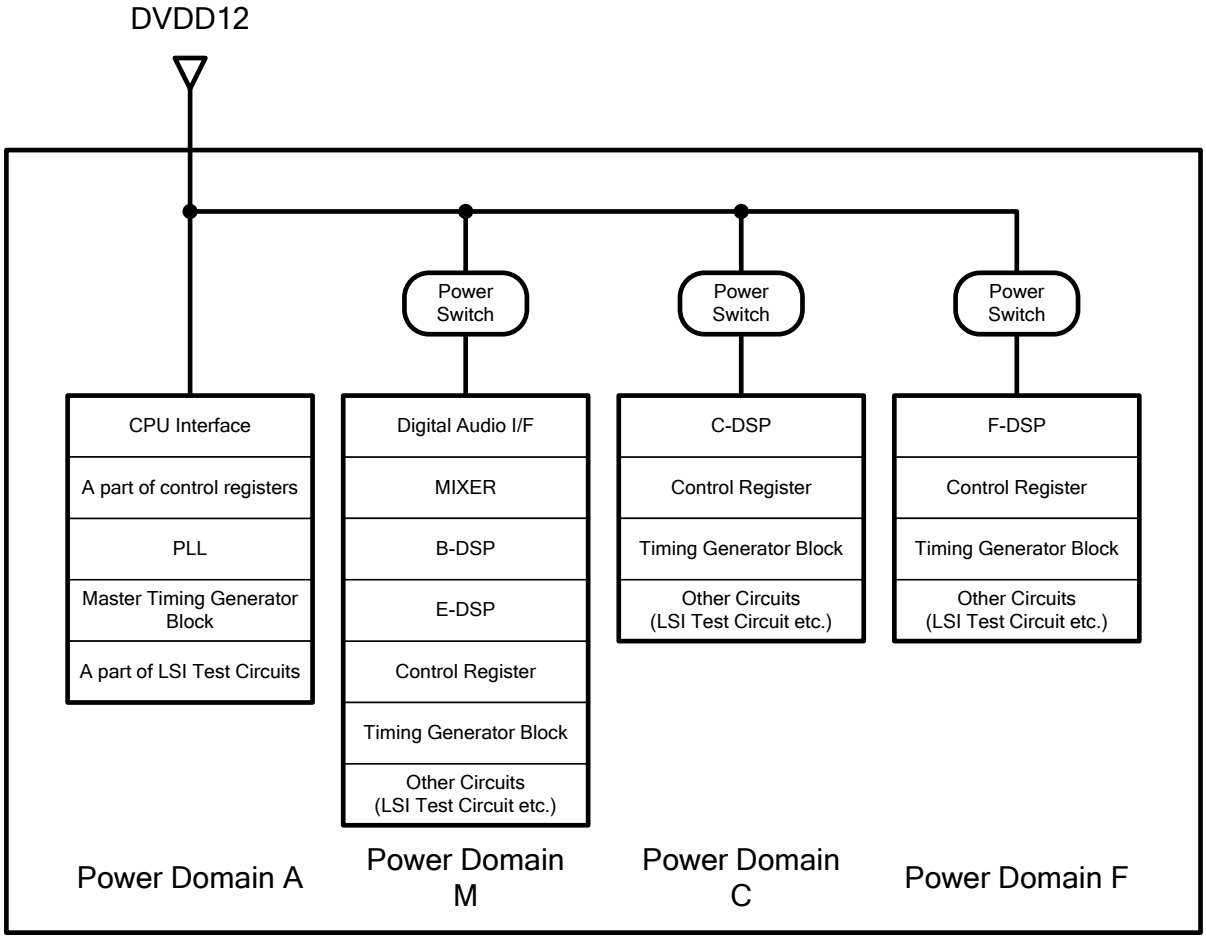
・LDOCP, LDOA, and LDO12 can be on and off with register values.

・LDO18 supplies power when VDD33 is supplied.
(LDO18 cannot be on and off with register values.)

See <*Figure 8 1. Single Supply Configuration.*> in *8.2 Recommended Operating Conditions* for power supply configurations.

6.2.2 Power Domains

1.2 V digital block has some DVDD12 power switches integrated, allowing for switching a part of the block on and off. The figure below shows the relationship between function blocks and power domains.



Power Domain A is always ON while DVDD12 is supplied, and *Power Domain [M / C / F]* can be powered on and off with power switches.

・Power Domain [C / F] can be powered off when not used.

・Power Domain M must be powered on when in operation.

See *7.4.2 Power Management* for details of setting power switches.

1.8 V digital block has no power switches (power domains).

6.2.3 Starting Device

6.2.3.1 SPI Master Mode (With On-chip MPU)

No.	Action	Description
P1-1	Power supply gets started	Keep MPURST_N “L” when the device starts getting power
P1-2	Device starts getting clock	Start supplying proper clock signal on CLKI pin
P1-3	Device getting out of reset state	Set MPURST_N to “H“ after CLKI clock becomes stable.

Eventually the embedded microcontroller starts running.

6.2.3.2 SPI Slave Mode (Without On-chip MPU)

No.	Action	Description
P1-1	Power supply gets started	
P1-2	Device starts getting clock	Start supplying proper clock signal on CLKI pin

6.3 Embedded Microcontroller

This device embedded a microcontroller which runs programs stored externally on the flash memory, and used for such tasks as exchanging data with the embedded DSPs, and controlling GPIO ports.
This embedded microcontroller runs only when the device is working as a master.

6.3.1 External Flash Memory Access

On startup, the microcontroller starts flash memory access with the following interface configuration.

SPI Mode	Mode 0
Bit Rate	CLKI frequency / (2^n) *1
Data Size	8 bits
Address Size	8/16/24 bits *2

*1. *n* is an integer 7 (the default) down to 1, and can be reconfigured with a parameter on the flash.
*2. The microcontroller determines the address size from a parameter on the flash, and performs the access properly with each size as follows.

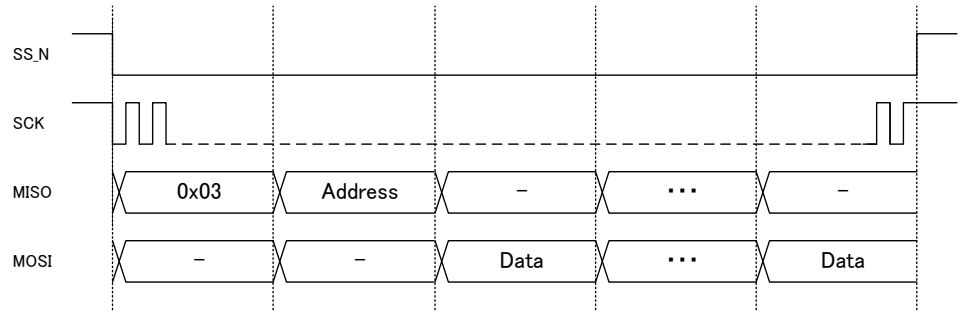


Figure 6-10. Interface timing chart (8-bit long).

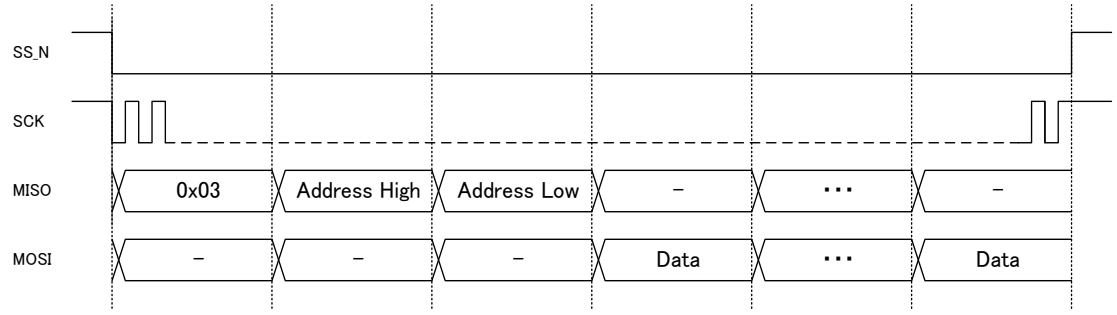


Figure 6-11. Interface timing chart (16-bit long).

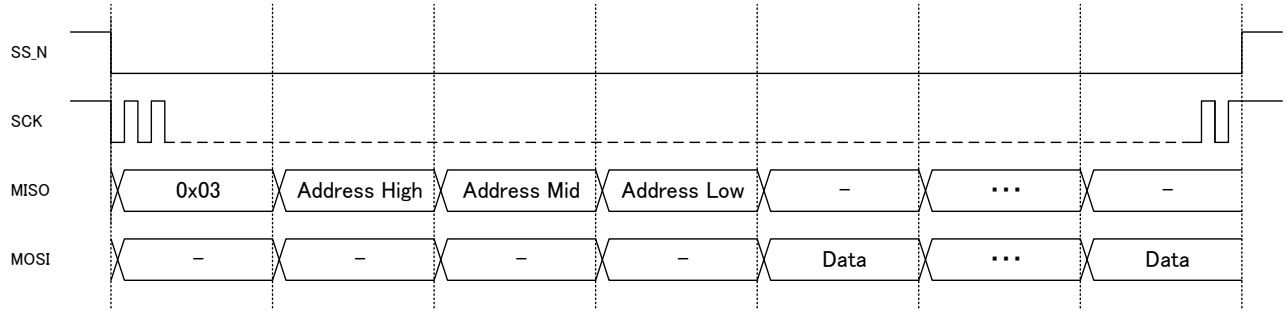


Figure 6-12. Interface timing chart (24-bit long).

SS_N, SCK, MISO, and MOSI pins enter the high-impedance states when both TEST1 and MPUE_N are "H". This can be used for on‑board programming of the flash memory.

6.3.2 Selecting DSP Data With GPI Pin Strapping

The different set of DSP data on the flash will be copied depending on how GPIO[0/1/2/3] is strapped.

6.3.3 Selecting GPO Pin Output

GPIO[0/1/2/3] pin output levels can be controlled with values on the flash.

6.3.4 I^2C Interface

The interface allows transmitting data to the embedded DSPs, controlling GPIO ports, etc.

6.4 Digital Microphone Interface (PDM)

YMU836 digital sound inputs support the pulse density modulation (PDM) format used by some microphones.
To use PDM, set PA[0/1/2]_* registers appropriately.
The relationship between the registers and the microphone interface pins is as follows:

PA0: DMCK
PA1: DMDIN0
PA2: DMDIN1

7 Register Descriptions

Descriptions in *7.1 Register Overview* and *7.2 Accessing Intermediate Registers* are those for operations in SPI slave mode.

7.1 Register Overview

The rest of the chapter describes how the device works in the slave mode.

Shown below are two kinds of registers, the *Interface Register* which the host can address directly on the bus and *Intermediate Registers* to which the host uses the Interface Register to get indirect access.

YMU836 uses the SPI bus interface for the device register access.

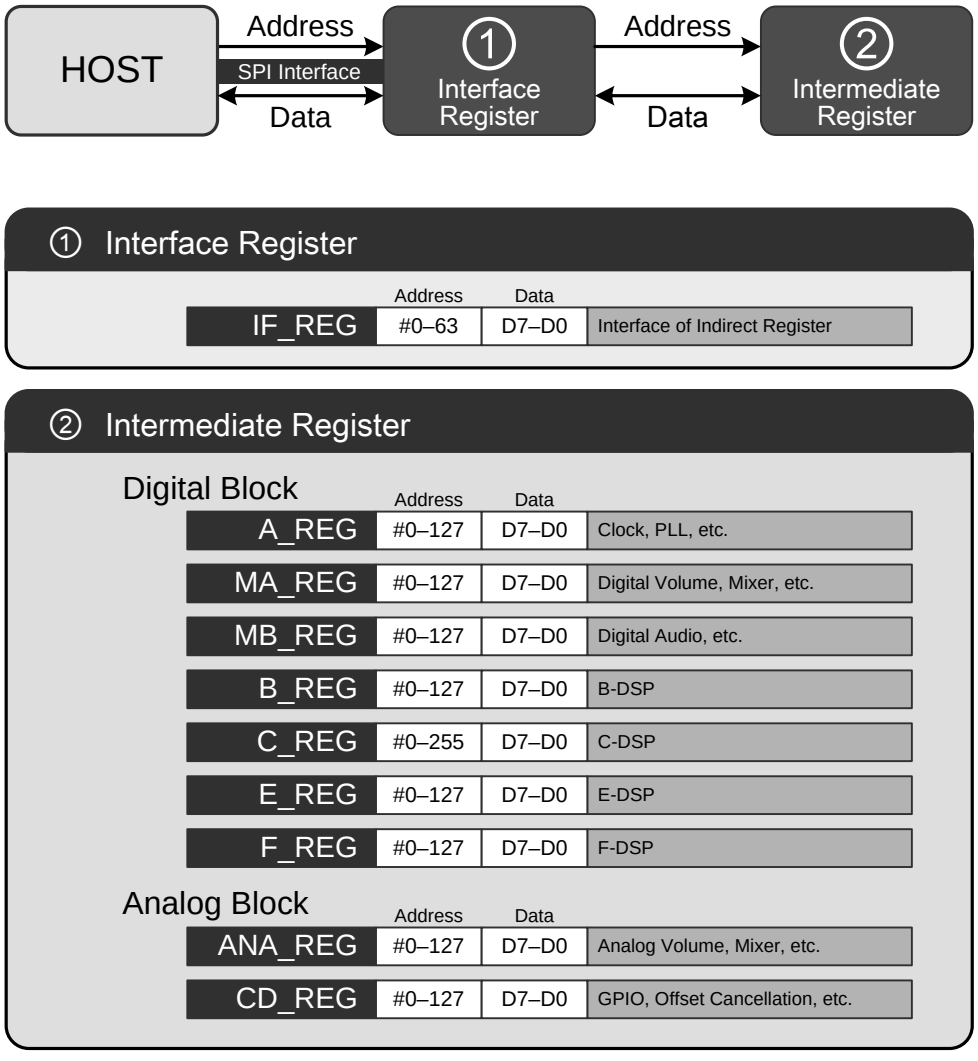


Figure 7-1. Register structure.

7.2 Accessing Intermediate Registers

*Intermediate Register*s are those registers accessed indirectly from the host controller through the *Interface Register*.

7.2.1 Burst Access Support to Intermediate Register Read/Write

Table 7.1. Burst Access Support to Intermediate Register Read/Write

Intermediate Register	BW	BR	Burst Write/Read *_REG_AINC				Address *_REG_A		Data *_REG_D	
			Name	WA	RA	IF_REG	Name	IF_REG	Name	IF_REG
A_REG	✓	✓	A_REG_AINC	✓	–	#0	A_REG_A	#0	A_REG_D	#1
MA_REG	✓	✓	MA_REG_AINC	✓	–	#12	MA_REG_A	#12	MA_REG_D	#13
MB_REG	✓	✓	MB_REG_AINC	✓	–	#14	MB_REG_A	#14	MB_REG_D	#15
B_REG	✓	✓	B_REG_AINC	✓	✓	#16	B_REG_A	#16	B_REG_D	#17
C_REG	✓	✓	–	–	–	–	C_REG_A	#40	C_REG_D	#41
E_REG	✓	✓	E_REG_AINC	✓	–	#32	E_REG_A	#32	E_REG_D	#33
F_REG	✓	✓	F_REG_AINC	✓	✓	#48	F_REG_A	#48	F_REG_D	#49
ANA_REG	✓	–	ANA_REG_AINC	✓	–	#6	ANA_REG_A	#6	ANA_REG_D	#7
CD_REG	✓	–	CD_REG_AINC	✓	–	#8	CD_REG_A	#8	CD_REG_D	#9

BW— Burst writes supported or not
BR— Burst reads supported or not
WA— Enable or disable automatic address pointer increment in burst writes
RA— Enable or disable automatic address pointer increment in burst reads

7.2.2 Writing Intermediate Registers

1. Set **_REG_AINC* to "1" when you enable the automatic address pointer increments.
2. Put *Intermediate Register* address to be written in **_REG_A*.
3. Put data in **_REG_D*. The address pointer in **_REG_A* is incremented by 1 after each writes with the automatic address pointer increment enabled.

7.2.3 Reading Intermediate Registers

1. Put *Intermediate Register* address to be read in **_REG_A*.
2. Read the data from **_REG_D*.

7.3 Register Map

7.3.1 IF_REG (Interface of intermediate Register)

IF_REG DEC	IF_REG HEX	Function	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#0	0x00	A_REG	W/R	A_REG_AINC	A_REG_A[6:0]						
#1	0x01	Access Window	W/R	A_REG_D[7:0]							
#2	0x02	Power/Reset Control	W/R	"0"	"0"	"0"	"0"	"0"	"0"	"0"	RST_A
#3	0x03		W	"1"	PSW_M_OFF	PSW_F_OFF	PSW_C_OFF	"1"	RST_M	RST_F	RST_C
			R	"1"	PSW_M_FLAG	PSW_F_FLAG	PSW_C_FLAG				
#4	0x04	Interrupt	W/R	"0"	"0"	"0"	"0"	"0"	"0"	IRQ	EIRQ
#6	0x06	ANA_REG	W/R	ANA_REG_AINC	ANA_REG_A[6:0]						
#7	0x07	Access Window	W/R	ANA_REG_D[7:0]							
#8	0x08	CD_REG	W/R	CD_REG_AINC	CD_REG_A[6:0]						
#9	0x09	Access Window	W/R	CD_REG_D[7:0]							
#10	0x0A	Interrupt	W/R	"0"	"0"	"0"	"0"	"0"	"0"	IRQR	EIRQR
#12	0x0C	B-DSP	W/R	MA_REG_AINC	MA_REG_A[6:0]						
#13	0x0D		W/R	MA_REG_D[7:0]							
#14	0x0E		W/R	MB_REG_AINC	MB_REG_A[6:0]						
#15	0x0F		W/R	MB_REG_D[7:0]							
#16	0x10		W/R	B_REG_AINC	B_REG_A[6:0]						
#17	0x11		W/R	B_REG_D[7:0]							
#18	0x12		W/R	"0"	"0"	"0"	"0"	"0"	"0"	"0"	BMAA[16]
#19	0x13		W/R	BMAA[15:8]							
#20	0x14		W/R	BMAA[7:0]							
#21	0x15		W/R	BDSPTINI	"0"	"0"	"0"	BMAMOD	BMADIR	BMABUS[1:0]	
#22	0x16		W/R	BMAD[7:0]							
#23	0x17		W/R	BDSPTREQ	"0"	"0"	"0"	"0"	"0"	"0"	"0"
#32	0x20	E-DSP	W/R	E_REG_AINC	E_REG_A[6:0]						
#33	0x21		W/R	E_REG_D[7:0]							
#34	0x22		W/R	EDSP_FW_PAGE[3:0]				"0"	"0"	"0"	EDSP_FW_A[8]
#35	0x23		W/R	EDSP_FW_A[7:0]							
#36	0x24		W/R	EDSP_FW_D[7:0]							
#37	0x25		W/R	"0"	"0"	"0"	EE2DSP_STA	"0"	"0"	"0"	EE1DSP_STA
#38	0x26		W/R	"0"	"0"	"0"	E2DSP_STA	"0"	"0"	"0"	E1DSP_STA
#40	0x28	C-DSP	W/R	C_REG_A[7:0]							
#41	0x29		W/R	C_REG_D[7:0]							
#42	0x2A		W	DEC_FIFO[7:0]							
			R	REC_FIFO[7:0]							
#43	0x2B		W/R	ECDSP	EFFIFO	ERFIFO	EEFIFO	EOFIFO	EDFIFO	EENC	EDEC
#44	0x2C		W/R	CDSP	FFIFO	RFIFO	EFIFO	OFIFO	DFIFO	ENC	DEC
#48	0x30	F-DSP	W/R	F_REG_AINC	F_REG_A[6:0]						
#49	0x31		W/R	F_REG_D[7:0]							
#50	0x32		W/R	"0"	"0"	"0"	"0"	FMAA[19:16]			
#51	0x33		W/R	FMAA[15:8]							
#52	0x34		W/R	FMAA[7:0]							
#53	0x35		W/R	FDSPTINI	"0"	"0"	"0"	FMAMOD	FMADIR	FMABUS[1:0]	
#54	0x36		W/R	FMAD[7:0]							
#55	0x37		W/R	FDSPTREQ	"0"	"0"	"0"	"0"	"0"	"0"	"0"
#57	0x39		W/R	IESERR	"0"	IEAMTBEG	IEAMTEND	IEFW[3:0]			
#58	0x3A		W/R	IRSERR	"0"	IRAMTBEG	IRAMTEND	IRFW[3:0]			

7.3.2 A_REG (Clock, PLL etc)

A_REG DEC	A_REG HEX	Function	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#0	0x00	Hardware ID	R	DevID					VerID		
#1	0x01	Clock Pin Control	W/R	"0"	"0"	"0"	"0"	"0"	"1"	"1"	CLKI_MSK
#2	0x02	Clock	W/R	PLL_PD	ANACLK_PD	PE_CLK_PD	PB_CLK_PD	PM_CLK_PD	PF_CLK_PD	PC_CLK_PD	VCOOUT_PD
#5	0x05	Pin Control	W/R	DO1_DRV	BCLK1_INV	BCLK1_MSK	BCLK1_DDR	LRCK1_MSK	LRCK1_DDR	SDIN1_MSK	SDO1_DDR
#6	0x06		W/R	DO2_DRV	BCLK2_INV	BCLK2_MSK	BCLK2_DDR	LRCK2_MSK	LRCK2_DDR	SDIN2_MSK	SDO2_DDR
#8	0x08		W/R	"0"	"0"	PDM1_DATA _DELAY	PDM0_DATA _DELAY	"0"	PCMOUT2 _HIZ	PCMOUT1 _HIZ	"0"
#9	0x09		W/R	PA0_OUT	"0"	PA0_DDR	PA0_DATA	"0"	PA0_OUTSEL	PA0_MSK	PA0_INV
#10	0x0A		W/R	"0"	"0"	PA1_DDR	PA1_DATA	"0"	PA1_OUTSEL	PA1_MSK	PA1_INV
#11	0x0B		W/R	"0"	"0"	PA2_DDR	PA2_DATA	"0"	PA2_OUTSEL	PA2_MSK	PA2_INV
#12	0x0C		W/R	DOA_DRV	"0"	"0"	"0"	"0"	"0"	"0"	"0"
#13	0x0D	Select Port Connection	W/R	"0"	"0"	"0"	"0"	"0"	LP0_FP[2:0]		
#14	0x0E		W/R	"0"	"0"	"0"	"0"	"0"	LP1_FP[2:0]		
#15	0x0F		W/R	"0"	"0"	"0"	"0"	"0"	LP2_FP[2:0]		
#16	0x10		W/R	"0"	"0"	"0"	"0"	"0"	LP3_FP[2:0]		
#19	0x13	Clock Frequency	W/R	FDSP_DIVR[1:0]		"0"	FREQ73M	"0"	CDSP_DIVR[2:0]		
#24	0x18	PLL	W/R	"0"	"0"	"0"	"0"	"0"	PLL_PS	"0"	PLL_INT
#25	0x19		W/R	"0"	"0"	PLL_PREDIV[5:0]					
#26	0x1A		W/R	"0"	"0"	PLL_FBDIV[13:8]					
#27	0x1B		W/R	PLL_FBDIV[7:0]							
#28	0x1C		W/R	PLL_FRAC[15:8]							
#29	0x1D		W/R	PLL_FRAC[7:0]							
#30	0x1E		W/R	"0"	"0"	"0"	"0"	"0"	"0"	PLL_FOUT	"0"

7.3.3 MA_REG (Digital volume Mixer etc.)

MA_REG DEC	MA_REG HEX	Function	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#0	0x00	Volume	R	DIFI3_VFLAG1	DIFI3_VFLAG0	DIFI2_VFLAG1	DIFI2_VFLAG0	DIFI1_VFLAG1	DIFI1_VFLAG0	DIFI0_VFLAG1	DIFI0_VFLAG0
#1	0x01		R	"0"	"0"	ADI2_VFLAG1	ADI2_VFLAG0	ADI1_VFLAG1	ADI1_VFLAG0	ADI0_VFLAG1	ADI0_VFLAG0
#2	0x02		R	DIFO3_VFLAG1	DIFO3_VFLAG0	DIFO2_VFLAG1	DIFO2_VFLAG0	DIFO1_VFLAG1	DIFO1_VFLAG0	DIFO0_VFLAG1	DIFO0_VFLAG0
#3	0x03		R	"0"	"0"	"0"	"0"	DAO1_VFLAG1	DAO1_VFLAG0	DAO0_VFLAG1	DAO0_VFLAG0
#4	0x04		W/R	"0"	ADI2_VINTP	ADI1_VINTP	ADI0_VINTP	DIFI3_VINTP	DIFI2_VINTP	DIFI1_VINTP	DIFI0_VINTP
#5	0x05		W/R	"0"	"0"	DAO1_VINTP	DAO0_VINTP	DIFO3_VINTP	DIFO2_VINTP	DIFO1_VINTP	DIFO0_VINTP
#6	0x06		W/R	DIFI0_VSEP	DIFI0_VOL0[6:0]						
#7	0x07		W/R	"0"	DIFI0_VOL1[6:0]						
#8	0x08		W/R	DIFI1_VSEP	DIFI1_VOL0[6:0]						
#9	0x09		W/R	"0"	DIFI1_VOL1[6:0]						
#10	0x0A		W/R	DIFI2_VSEP	DIFI2_VOL0[6:0]						
#11	0x0B		W/R	"0"	DIFI2_VOL1[6:0]						
#12	0x0C		W/R	DIFI3_VSEP	DIFI3_VOL0[6:0]						
#13	0x0D		W/R	"0"	DIFI3_VOL1[6:0]						
#14	0x0E		W/R	ADI0_VSEP	ADI0_VOL0[6:0]						
#15	0x0F		W/R	"0"	ADI0_VOL1[6:0]						
#16	0x10		W/R	ADI1_VSEP	ADI1_VOL0[6:0]						
#17	0x11		W/R	"0"	ADI1_VOL1[6:0]						
#18	0x12		W/R	ADI2_VSEP	ADI2_VOL0[6:0]						
#19	0x13		W/R	"0"	ADI2_VOL1[6:0]						
#20	0x14		W/R	DIFO0_VSEP	DIFO0_VOL0[6:0]						
#21	0x15		W/R	"0"	DIFO0_VOL1[6:0]						
#22	0x16		W/R	DIFO1_VSEP	DIFO1_VOL0[6:0]						
#23	0x17		W/R	"0"	DIFO1_VOL1[6:0]						
#24	0x18		W/R	DIFO2_VSEP	DIFO2_VOL0[6:0]						
#25	0x19		W/R	"0"	DIFO2_VOL1[6:0]						
#26	0x1A		W/R	DIFO3_VSEP	DIFO3_VOL0[6:0]						
#27	0x1B		W/R	"0"	DIFO3_VOL1[6:0]						
#28	0x1C		W/R	DAO0_VSEP	DAO0_VOL0[6:0]						
#29	0x1D		W/R	"0"	DAO0_VOL1[6:0]						
#30	0x1E		W/R	DAO1_VSEP	DAO1_VOL0[6:0]						
#31	0x1F		W/R	"0"	DAO1_VOL1[6:0]						
#32	0x20	Swap	W/R	"0"	ADI1_SWAP[2:0]			"0"	ADI0_SWAP[2:0]		
#33	0x21		W/R	"0"	"0"	"0"	"0"	"0"	ADI2_SWAP[2:0]		
#34	0x22		W/R	"0"	DAO1_SWAP[2:0]			"0"	DAO0_SWAP[2:0]		
#35	0x23	Mixer	W/R	IN0_MSEP	IN0_MIX0[6:0]						
#36	0x24		W/R	"0"	IN0_MIX1[6:0]						
#37	0x25		W/R	IN1_MSEP	IN1_MIX0[6:0]						
#38	0x26		W/R	"0"	IN1_MIX1[6:0]						
#39	0x27		W/R	IN2_MSEP	IN2_MIX0[6:0]						
#40	0x28		W/R	"0"	IN2_MIX1[6:0]						
#41	0x29		W/R	IN3_MSEP	IN3_MIX0[6:0]						
#42	0x2A		W/R	"0"	IN3_MIX1[6:0]						
#43	0x2B		W/R	OUT0_MSEP	"0"	"0"	"0"	"0"	OUT0_MIX0[10:8]		
#44	0x2C		W/R	OUT0_MIX0[7:0]							
#45	0x2D		W/R	"0"	"0"	"0"	"0"	"0"	OUT0_MIX1[10:8]		
#46	0x2E		W/R	OUT0_MIX1[7:0]							
#47	0x2F		W/R	OUT1_MSEP	"0"	"0"	"0"	"0"	OUT1_MIX0[10:8]		
#48	0x30		W/R	OUT1_MIX0[7:0]							
#49	0x31		W/R	"0"	"0"	"0"	"0"	"0"	OUT1_MIX1[10:8]		
#50	0x32		W/R	OUT1_MIX1[7:0]							
#51	0x33		W/R	OUT2_MSEP	"0"	"0"	"0"	"0"	OUT2_MIX0[10:8]		
#52	0x34		W/R	OUT2_MIX0[7:0]							
#53	0x35		W/R	"0"	"0"	"0"	"0"	"0"	OUT2_MIX1[10:8]		
#54	0x36		W/R	OUT2_MIX1[7:0]							
#55	0x37		W/R	OUT3_MSEP	"0"	"0"	"0"	"0"	OUT3_MIX0[10:8]		
#56	0x38		W/R	OUT3_MIX0[7:0]							
#57	0x39		W/R	"0"	"0"	"0"	"0"	"0"	OUT3_MIX1[10:8]		
#58	0x3A		W/R	OUT3_MIX1[7:0]							
#59	0x3B		W/R	OUT4_MSEP	"0"	"0"	"0"	"0"	OUT4_MIX0[10:8]		
#60	0x3C		W/R	OUT4_MIX0[7:0]							
#61	0x3D		W/R	"0"	"0"	"0"	"0"	"0"	OUT4_MIX1[10:8]		
#62	0x3E		W/R	OUT4_MIX1[7:0]							
#63	0x3F		W/R	OUT5_MSEP	"0"	"0"	"0"	"0"	OUT5_MIX0[10:8]		
#64	0x40		W/R	OUT5_MIX0[7:0]							
#65	0x41		W/R	"0"	"0"	"0"	"0"	"0"	OUT5_MIX1[10:8]		
#66	0x42		W/R	OUT5_MIX1[7:0]							
#67	0x43	M-DSP	W/R	DSP_ERR	"0"	"0"	"0"	"0"	"0"	"0"	DSP_START
#68	0x44		W/R	SPATH_ON	IN_MIX_ON	OUT_MIX_ON[5:0]					
#71	0x47	Volume	W/R	LINK_LOCK	"0"	"0"	"0"	"0"	"0"	"0"	"0"
#80	0x50	Switch	W/R	FDSP_EX_SYNC	"0"	"0"	"0"	FDSP_PI_SOURCE[3:0]			
#81	0x51		W/R	"0"	"0"	FDSP_PO_SOURCE[5:0]					
#82	0x52		W/R	AE_PO3 _SOURCE	AE_PO2 _SOURCE	AE_PO1 _SOURCE	AE_PO0 _SOURCE	"0"	"0"	BDSP_PI1 _SOURCE	BDSP_PI0 _SOURCE
#83	0x53		W/R	"0"	"0"	LPT2 _VSOURCE	ISRC3 _VSOURCE	ISRC2_CH1 _VSOURCE	ISRC2 _VSOURCE	SRC3_CTRL[1:0]	
#84	0x54		W/R	"0"	"0"	LPT2_MIX_VOLO[1:0]		"0"	"0"	LPT2_MIX_VOLI[1:0]	

7.3.4 MB_REG (Digital audio etc.)

MB_REG DEC	MB_REG HEX	Function	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#0	0x00	Digital Audio #0	W/R	LPT0_STMODE	LP0_AUTO_FS	"0"	LPT0_EDGE	LP0_CH[1:0]		"0"	LP0_MODE
#1	0x01		W/R	LP0_BCK[3:0]				LP0_FS[3:0]			
#2	0x02		W/R	"0"	"0"	LPR0_P2_SLOT[1:0]		LPR0_P1_SLOT[1:0]		LPR0_P0_SLOT[1:0]	
#3	0x03		W/R	"0"	"0"	LPR0_P2_SWAP[1:0]		LPR0_P1_SWAP[1:0]		LPR0_P0_SWAP[1:0]	
#4	0x04		W/R	"0"	"0"	LPT0_P2_SLOT[1:0]		LPT0_P1_SLOT[1:0]		LPT0_P0_SLOT[1:0]	
#5	0x05		W/R	"0"	LPT0_P2_SWAP[1:0]		LPT0_P1_SWAP[1:0]		LPT0_P0_SWAP[2:0]		
#6	0x06		W/R	LPT0_FMT[1:0]		LPT0_BIT[1:0]		LPR0_FMT[1:0]		LPR0_BIT[1:0]	
#7	0x07		W/R	LPT0_HIZ_REDGE	"0"	LP0_PCM_FRAME	LP0_PCM_HPERIOD[4:0]				
#8	0x08		W/R	LPR0_PCM_MONO	"0"	"0"	LPR0_PCM_LSBON	LPR0_PCM_LAW[1:0]		LPR0_PCM_BIT[1:0]	
#9	0x09		W/R	LPT0_PCM_MONO	"0"	"0"	LPT0_PCM_LSBON	LPT0_PCM_LAW[1:0]		LPT0_PCM_BIT[1:0]	
#10	0x0A		W/R	LP0_TIM_START	"0"	LPR0_STOP_EN	LPT0_STOP_EN	LPR0_START[1:0]		LPT0_START[1:0]	
#16	0x10	Digital Audio #1	W/R	LPT1_STMODE	LP1_AUTO_FS	"0"	LPT1_EDGE	"0"	"0"	"0"	LP1_MODE
#17	0x11		W/R	LP1_BCK[3:0]				LP1_FS[3:0]			
#19	0x13		W/R	"0"	"0"	"0"	"0"	"0"	"0"	LPR1_P0_SWAP[1:0]	
#21	0x15		W/R	"0"	"0"	"0"	"0"	"0"	"0"	LPT1_P0_SWAP[1:0]	
#22	0x16		W/R	LPT1_FMT[1:0]		LPT1_BIT[1:0]		LPR1_FMT[1:0]		LPR1_BIT[1:0]	
#23	0x17		W/R	LPT1_HIZ_REDGE	"0"	LP1_PCM_FRAME	LP1_PCM_HPERIOD[4:0]				
#24	0x18		W/R	LPR1_PCM_MONO	"0"	"0"	LPR1_PCM_LSBON	LPR1_PCM_LAW[1:0]		LPR1_PCM_BIT[1:0]	
#25	0x19		W/R	LPT1_PCM_MONO	"0"	"0"	LPT1_PCM_LSBON	LPT1_PCM_LAW[1:0]		LPT1_PCM_BIT[1:0]	
#26	0x1A		W/R	LP1_TIM_START	"0"	LPR1_STOP_EN	LPRT1_STOP_EN	LPR1_START[1:0]		LPT1_START[1:0]	
#32	0x20	Digital Audio #2	W/R	LPT2_STMODE	LP2_AUTO_FS	"0"	LPT2_EDGE	"0"	"0"	"0"	LP2_MODE
#33	0x21		W/R	LP2_BCK[3:0]				LP2_FS[3:0]			
#35	0x23		W/R	"0"	"0"	"0"	"0"	"0"	"0"	LPR2_P0_SWAP[1:0]	
#37	0x25		W/R	"0"	"0"	"0"	"0"	"0"	"0"	LPT2_P0_SWAP[1:0]	
#38	0x26		W/R	LPT2_FMT[1:0]		LPT2_BIT[1:0]		LPR2_FMT[1:0]		LPR2_BIT[1:0]	
#39	0x27		W/R	LPT2_HIZ_REDGE	"0"	LP2_PCM_FRAME	LP2_PCM_HPERIOD[4:0]				
#40	0x28		W/R	LPR2_PCM_MONO	"0"	"0"	LPR2_PCM_LSBON	LPR2_PCM_LAW[1:0]		LPR2_PCM_BIT[1:0]	
#41	0x29		W/R	LPT2_PCM_MONO	"0"	"0"	LPT2_PCM_LSBON	LPT2_PCM_LAW[1:0]		LPT2_PCM_BIT[1:0]	
#42	0x2A		W/R	LP2_TIM_START	"0"	LPR2_STOP_EN	LPT2_STOP_EN	LPR2_START[1:0]		LPT2_START[1:0]	
#43	0x2B	ASRC#3	W/R	"0"	"0"	"0"	SRC3_THRU	SRC3_FS[3:0]			
#44	0x2C		W/R	SRC3_TIM_START	"0"	"0"	"0"	ISRC3 _START	"0"	OSRC3 _START	"0"
#48	0x30	Digital Audio #3	W/R	LPT3_STMODE	"0"	"0"	LPT3_EDGE	"0"	"0"	"0"	"0"
#49	0x31		W/R	"0"	"0"	LP3_BCK[1:0]		LP3_FS[3:0]			
#51	0x33		W/R	"0"	"0"	"0"	"0"	"0"	"0"	LPR3_P0_SWAP[1:0]	
#53	0x35		W/R	"0"	"0"	"0"	"0"	"0"	"0"	LPT3_P0_SWAP[1:0]	
#54	0x36		W/R	LPT3_FMT[1:0]		LPT3_BIT[1:0]		LPR3_FMT[1:0]		LPR3_BIT[1:0]	
#58	0x3A		W/R	LP3_TIM_START	"0"	"0"	"0"	LPR3 _STOP_EN	LPR3 _START	LPT3 _STOP_EN	LPT3 _START
#85	0x55	Digital Audio	W/R	T_DPLL_FAST	VOLREL_TIME[1:0]		"0"	"0"	"0"	"0"	"0"

7.3.5 B_REG (B-DSP)

B_REG		Function	W/R	D7	D6	D5	D4	D3	D2	D1	D0
DEC	HEX										
#0	0x00	B-DSP	W/R	BDSPBYPASS	"0"	"0"	"0"	"0"	"0"	"0"	BDSPSTART
#64	0x40	Firmware Control	W/R	BFWCTL0[7:0]							
#65	0x41		W/R	BFWCTL1[7:0]							
#66	0x42		W/R	BFWCTL2[7:0]							
#67	0x43		W/R	BFWCTL3[7:0]							
#68	0x44		W/R	BFWCTL4[7:0]							
#69	0x45		W/R	BFWCTL5[7:0]							
#70	0x46		W/R	BFWCTL6[7:0]							
#71	0x47		W/R	BFWCTL7[7:0]							

7.3.6 C_REG (C-DSP)

C_REG DEC	C_REG HEX	Function	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#0	0x00	C-DSP	W/R	CDSP_SAVEOFF	"0"	"0"	"0"	"0"	"0"	"0"	"0"
#1	0x01		R	OFIFO_LVL[3:0]				DFIFO_LVL[3:0]			
#2	0x02		R	RFIFO_LVL[3:0]				EFIFO_LVL[3:0]			
#3	0x03		R	"0"	"0"	"0"	"0"	FFIFO_LVL[3:0]			
#4	0x04		R	DEC_POS[31:24]							
#5	0x05		R	DEC_POS[23:16]							
#6	0x06		R	DEC_POS[15:8]							
#7	0x07		W/R	DEC_POS[7:0]							
#8	0x08		R	ENC_POS[31:24]							
#9	0x09		R	ENC_POS[23:16]							
#10	0x0A		R	ENC_POS[15:8]							
#11	0x0B		W/R	ENC_POS[7:0]							
#12	0x0C		R	DEC_ERR[7:0]							
#13	0x0D		R	ENC_ERR[7:0]							
#14	0x0E		W/R	"0"	"0"	"0"	FFIFO_RST	EFIFO_RST	RFIFO_RST	OFIFO_RST	DFIFO_RST
#15	0x0F		W/R	OUT_START_SEL	"0"	"0"	FSQ_START	ENC_START	CDSP_OUT_START	OUT_START	DEC_START
#16	0x10		W/R	EFIFO_START_SEL	EFIFO_START	EFIFO_CH[1:0]		CDSP_EFIFO_START	"0"	OFIFO_CH[1:0]	
#17	0x11		W/R	RFIFO_START_SEL	"0"	"0"	"0"	"0"	CDSP_RFIFO_START	RFIFO_START	"0"
#19	0x13	C-DSP	W/R	DEC_CTL15[7:0]							
#20	0x14		W/R	DEC_CTL14[7:0]							
#21	0x15		W/R	DEC_CTL13[7:0]							
#22	0x16		W/R	DEC_CTL12[7:0]							
#23	0x17		W/R	DEC_CTL11[7:0]							
#24	0x18		W/R	DEC_CTL10[7:0]							
#25	0x19		W/R	DEC_CTL9[7:0]							
#26	0x1A		W/R	DEC_CTL8[7:0]							
#27	0x1B		W/R	DEC_CTL7[7:0]							
#28	0x1C		W/R	DEC_CTL6[7:0]							
#29	0x1D		W/R	DEC_CTL5[7:0]							
#30	0x1E		W/R	DEC_CTL4[7:0]							
#31	0x1F		W/R	DEC_CTL3[7:0]							
#32	0x20		W/R	DEC_CTL2[7:0]							
#33	0x21		W/R	DEC_CTL1[7:0]							
#34	0x22		W/R	DEC_CTL0[7:0]							
#35	0x23	C-DSP	R	DEC_GPR15[7:0]							
#36	0x24		R	DEC_GPR14[7:0]							
#37	0x25		R	DEC_GPR13[7:0]							
#38	0x26		R	DEC_GPR12[7:0]							
#39	0x27		R	DEC_GPR11[7:0]							
#40	0x28		R	DEC_GPR10[7:0]							
#41	0x29		R	DEC_GPR9[7:0]							
#42	0x2A		R	DEC_GPR8[7:0]							
#43	0x2B		R	DEC_GPR7[7:0]							
#44	0x2C		R	DEC_GPR6[7:0]							
#45	0x2D		R	DEC_GPR5[7:0]							
#46	0x2E		R	DEC_GPR4[7:0]							
#47	0x2F		R	DEC_GPR3[7:0]							
#48	0x30		R	DEC_GPR2[7:0]							
#49	0x31		R	DEC_GPR1[7:0]							
#50	0x32		R	DEC_GPR0[7:0]							
#51	0x33	C-DSP	W/R	DEC_SFR1[7:0]							
#52	0x34		W/R	DEC_SFR0[7:0]							
#53	0x35	C-DSP	W/R	ENC_CTL15[7:0]							
#54	0x36		W/R	ENC_CTL14[7:0]							
#55	0x37		W/R	ENC_CTL13[7:0]							
#56	0x38		W/R	ENC_CTL12[7:0]							
#57	0x39		W/R	ENC_CTL11[7:0]							
#58	0x3A		W/R	ENC_CTL10[7:0]							
#59	0x3B		W/R	ENC_CTL9[7:0]							
#60	0x3C		W/R	ENC_CTL8[7:0]							
#61	0x3D		W/R	ENC_CTL7[7:0]							
#62	0x3E		W/R	ENC_CTL6[7:0]							
#63	0x3F		W/R	ENC_CTL5[7:0]							
#64	0x40		W/R	ENC_CTL4[7:0]							
#65	0x41		W/R	ENC_CTL3[7:0]							
#66	0x42		W/R	ENC_CTL2[7:0]							
#67	0x43		W/R	ENC_CTL1[7:0]							
#68	0x44		W/R	ENC_CTL0[7:0]							
#69	0x45	C-DSP	R	ENC_GPR15[7:0]							
#70	0x46		R	ENC_GPR14[7:0]							
#71	0x47		R	ENC_GPR13[7:0]							
#72	0x48		R	ENC_GPR12[7:0]							
#73	0x49		R	ENC_GPR11[7:0]							
#74	0x4A		R	ENC_GPR10[7:0]							
#75	0x4B		R	ENC_GPR9[7:0]							
#76	0x4C		R	ENC_GPR8[7:0]							
#77	0x4D		R	ENC_GPR7[7:0]							
#78	0x4E		R	ENC_GPR6[7:0]							
#79	0x4F		R	ENC_GPR5[7:0]							
#80	0x50		R	ENC_GPR4[7:0]							
#81	0x51		R	ENC_GPR3[7:0]							
#82	0x52		R	ENC_GPR2[7:0]							
#83	0x53		R	ENC_GPR1[7:0]							
#84	0x54		R	ENC_GPR0[7:0]							
#85	0x55	C-DSP	W/R	ENC_SFR1[7:0]							
#86	0x56		W/R	ENC_SFR0[7:0]							

7.3.7 E_REG (E-DSP)

E_REG DEC	E_REG HEX	Function	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#0	0x00	E1DSP	W/R	"0"	"0"	"0"	"0"	"0"	"0"	"0"	E1DSP_RST
#1	0x01	E1DSP	W	E1COMMAND[7:0]							
			R	E1STATUS[7:0]							
#2	0x02	LPF / OSF	W/R	LPF1 _PST_THR	LPF0 _PST_THR	LPF1 _PRE_THR	LPF0 _PRE_THR	OSF1_MN	OSF0_MN	OSF1_ENB	OSF0_ENB
#3	0x03	DC Cut	W/R	"0"	"0"	"0"	"0"	DAC_DCC1_SEL[1:0]		DAC_DCC0_SEL[1:0]	
#8	0x08	OSF	W/R	"0"	"0"	"0"	"0"	OSF1_SEL[1:0]		OSF0_SEL[1:0]	
#28	0x1C	Direct Path	W/R	"0"	"0"	"0"	"0"	"0"	DIRECT _ENB_ADC	DIRECT _ENB_DAC1	DIRECT _ENB_DAC0
#29	0x1D	Direct Path	W/R	"0"	"0"	"0"	"0"	"0"	"0"	DPATH _DA_VFLAG	DPATH _DA_VINTP
#30	0x1E	Direct Path	W/R	DPATH_DA_VSEP	DPATH_DA_VOL_L[6:0]						
#31	0x1F	Direct Path	W/R	"0"	DPATH_DA_VOL_R[6:0]						
#32	0x20	Direct Path	W/R	"0"	"0"	"0"	"0"	"0"	"0"	DPATH _AD_VFLAG	DPATH _AD_VINTP
#33	0x21	Direct Path	W/R	DPATH_AD_VSEP	DPATH_AD_VOL_L[6:0]						
#34	0x22	Direct Path	W/R	"0"	DPATH_AD_VOL_R[6:0]						
#41	0x29	Decimation Filter	W/R	DSF0R_PRE_FLT_TYPE[1:0]		DSF0L_PRE_FLT_TYPE[1:0]		"0"	"0"	DSF0_MN	DSF0_ENB
#42	0x2A	Decimation Filter	W/R	"0"	DSF0R_PRE_INPUT[2:0]			"0"	DSF0L_PRE_INPUT[2:0]		
#42	0x2B	Decimation Filter	W/R	"0"	DSF1R_PRE _FLT_TYPE	"0"	DSF1L_PRE _FLT_TYPE	"0"	"0"	DSF1_MN	DSF1_ENB
#44	0x2C	Decimation Filter	W/R	"0"	DSF1R_PRE_INPUT[2:0]			"0"	DSF1L_PRE_INPUT[2:0]		
#45	0x2D	Decimation Filter	W/R	"0"	DSF2R_PRE _FLT_TYPE	"0"	DSF2L_PRE _FLT_TYPE	REF_SEL	REF_BACK	DSF2_MN	DSF2_ENB
#46	0x2E	Decimation Filter	W/R	"0"	DSF2R_PRE_INPUT[2:0]			"0"	DSF2L_PRE_INPUT[2:0]		
#47	0x2F	Decimation Filter	W/R	"0"	"0"	"0"	"0"	"0"	DSF2_SEL	DSF1_SEL	DSF0_SEL
#48	0x30	DC Cut	W/R	"0"	"0"	ADC_DCC2_SEL[1:0]		ADC_DCC1_SEL[1:0]		ADC_DCC0_SEL[1:0]	
#68	0x44	De-Pop	W/R	"0"	"0"	"0"	"0"	DEPOP0_WAIT[1:0]		DEPOP0_ATT[1:0]	
#69	0x345	De-Pop	W/R	"0"	"0"	"0"	"0"	DEPOP1_WAIT[1:0]		DEPOP1_ATT[1:0]	
#70	0x46	De-Pop	W/R	"0"	"0"	"0"	"0"	DEPOP2_WAIT[1:0]		DEPOP2_ATT[1:0]	
#71	0x47	PDM Interface	W/R	"0"	"0"	"0"	"0"	PDM_STWAIT[1:0]		PDM_MODE[1:0]	
#72	0x48	PDM Interface	W/R	PDM1_START	PDM1_LOAD_TIM[2:0]			PDM0_START	PDM0_LOAD_TIM[2:0]		
#73	0x49	PDM Interface	W/R	"0"	"0"	PDM0L_FINE_DLY[5:0]					
#74	0x4A	PDM Interface	W/R	"0"	"0"	PDM0R_FINE_DLY[5:0]					
#75	0x4B	PDM Interface	W/R	"0"	"0"	PDM1L_FINE_DLY[5:0]					
#76	0x4C	PDM Interface	W/R	"0"	"0"	PDM1R_FINE_DLY[5:0]					
#77	0x4D	E2DSP	W/R	"0"	"0"	"0"	"0"	"0"	"0"	"0"	E2DSP_RST
#78	0x4E	E2DSP	W	E2REQ_0[7:0]							
		E2DSP	R	E2RES_0[7:0]							
#79	0x4F	E2DSP	W	E2REQ_1[7:0]							
		E2DSP	R	E2RES_1[7:0]							
#80	0x50	E2DSP	W	E2REQ_2[7:0]							
		E2DSP	R	E2RES_2[7:0]							
#81	0x51	E2DSP	W	E2REQ_3[7:0]							
		E2DSP	R	E2RES_3[7:0]							
#82	0x52	E2DSP	W	E2REQ_4[7:0]							
		E2DSP	R	E2RES_4[7:0]							
#83	0x53	E2DSP	W	E2REQ_5[7:0]							
		E2DSP	R	E2RES_5[7:0]							
#84	0x54	E2DSP	W	E2REQ_6[7:0]							
		E2DSP	R	E2RES_6[7:0]							
#85	0x55	E2DSP	W	E2REQ_7[7:0]							
		E2DSP	R	E2RES_7[7:0]							
#86	0x56	E2DSP	W	E2COMMAND[7:0]							
		E2DSP	R	E2STATUS[7:0]							
#87	0x57	Path Control	W/R	"0"	"0"	"0"	"0"	"0"	"0"	LOOPBACK[1:0]	
#94	0x5E	Path Control	W/R	"0"	"0"	"0"	E2_DA_SEL[1:0]		E2_AD_SEL[2:0]		

7.3.8 F_REG (F-DSP)

F_REG DEC	F_REG HEX	Function	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#3	0x03	F-DSP	W/R	ADI3DFMT[1:0]		ADI2DFMT[1:0]		ADI1DFMT[1:0]		ADI0DFMT[1:0]	
#4	0x04		W/R	ADI7DFMT[1:0]		ADI6DFMT[1:0]		ADI5DFMT[1:0]		ADI4DFMT[1:0]	
#5	0x05		W/R	ADI07MTN	ADI06MTN	ADI05MTN	ADI04MTN	ADI03MTN	ADI02MTN	ADI01MTN	ADI00MTN
#6	0x06		W/R	ADI15MTN	ADI14MTN	ADI13MTN	ADI12MTN	ADI11MTN	ADI10MTN	ADI09MTN	ADI08MTN
#7	0x07		W	"0"	"0"	"0"	"0"	"0"	"0"	"0"	ADIMTSET
#8	0x08		W/R	ADI01CSEL[3:0]				ADI00CSEL[3:0]			
#9	0x09		W/R	ADI03CSEL[3:0]				ADI02CSEL[3:0]			
#10	0x0A		W/R	ADI05CSEL[3:0]				ADI04CSEL[3:0]			
#11	0x0B		W/R	ADI07CSEL[3:0]				ADI06CSEL[3:0]			
#12	0x0C		W/R	ADI09CSEL[3:0]				ADI08CSEL[3:0]			
#13	0x0D		W/R	ADI11CSEL[3:0]				ADI10CSEL[3:0]			
#14	0x0E		W/R	ADI13CSEL[3:0]				ADI12CSEL[3:0]			
#15	0x0F		W/R	ADI15CSEL[3:0]				ADI14CSEL[3:0]			
#19	0x13	F-DSP	W/R	ADO3DFMT[1:0]		ADO2DFMT[1:0]		ADO1DFMT[1:0]		ADO0DFMT[1:0]	
#20	0x14		W/R	ADO7DFMT[1:0]		ADO6DFMT[1:0]		ADO5DFMT[1:0]		ADO4DFMT[1:0]	
#21	0x15		W/R	ADO07MTN	ADO06MTN	ADO05MTN	ADO04MTN	ADO03MTN	ADO02MTN	ADO01MTN	ADO00MTN
#22	0x16		W/R	ADO15MTN	ADO14MTN	ADO13MTN	ADO12MTN	ADO11MTN	ADO10MTN	ADO09MTN	ADO08MTN
#23	0x17		W	"0"	"0"	"0"	"0"	"0"	"0"	"0"	ADOMTSET
#24	0x18		W/R	ADO01CSEL[3:0]				ADO00CSEL[3:0]			
#25	0x19		W/R	ADO03CSEL[3:0]				ADO02CSEL[3:0]			
#26	0x1A		W/R	ADO05CSEL[3:0]				ADO04CSEL[3:0]			
#27	0x1B		W/R	ADO07CSEL[3:0]				ADO06CSEL[3:0]			
#28	0x1C		W/R	ADO09CSEL[3:0]				ADO08CSEL[3:0]			
#29	0x1D		W/R	ADO11CSEL[3:0]				ADO10CSEL[3:0]			
#30	0x1E		W/R	ADO13CSEL[3:0]				ADO12CSEL[3:0]			
#31	0x1F		W/R	ADO15CSEL[3:0]				ADO14CSEL[3:0]			
#32	0x20		W/R	FDSPBYPASS	"0"	"0"	"0"	"0"	"0"	"0"	FDSPSTART
#33	0x21		R	AUTOMTN	"0"	"0"	"0"	"0"	"0"	"0"	DSPACT
#34	0x22		R	ADIFS[15:8]							
#35	0x23		R	ADIFS[7:0]							
#36	0x24		R	ADOFS[15:8]							
#37	0x25		R	ADOFS[7:0]							
#38	0x26		W/R	IRAPP[23:16]							
#39	0x27		W/R	IRAPP[15:8]							
#40	0x28		W/R	IRAPP[7:0]							
#41	0x29		W/R	IRTOP[7:0]							
#64	0x40	F-DSP	W/R	FFWCTL00[7:0]							
#65	0x41		W/R	FFWCTL01[7:0]							
#66	0x42		W/R	FFWCTL02[7:0]							
#67	0x43		W/R	FFWCTL03[7:0]							
#68	0x44		W/R	FFWCTL04[7:0]							
#69	0x45		W/R	FFWCTL05[7:0]							
#70	0x46		W/R	FFWCTL06[7:0]							
#71	0x47		W/R	FFWCTL07[7:0]							
#72	0x48		W/R	FFWCTL08[7:0]							
#73	0x49		W/R	FFWCTL09[7:0]							
#74	0x4A		W/R	FFWCTL10[7:0]							
#75	0x4B		W/R	FFWCTL11[7:0]							
#76	0x4C		W/R	FFWCTL12[7:0]							
#77	0x4D		W/R	FFWCTL13[7:0]							
#78	0x4E		W/R	FFWCTL14[7:0]							
#79	0x4F		W/R	FFWCTL15[7:0]							
#80	0x50		W/R	FFWCTL16[7:0]							
#81	0x51		W/R	FFWCTL17[7:0]							
#82	0x52		W/R	FFWCTL18[7:0]							
#83	0x53		W/R	FFWCTL19[7:0]							
#84	0x54		W/R	FFWCTL20[7:0]							
#85	0x55		W/R	FFWCTL21[7:0]							
#86	0x56		W/R	FFWCTL22[7:0]							
#87	0x57		W/R	FFWCTL23[7:0]							
#88	0x58		W/R	FFWCTL24[7:0]							
#89	0x59		W/R	FFWCTL25[7:0]							
#90	0x5A		W/R	FFWCTL26[7:0]							
#91	0x5B		W/R	FFWCTL27[7:0]							
#92	0x5C		W/R	FFWCTL28[7:0]							
#93	0x5D		W/R	FFWCTL29[7:0]							
#94	0x5E		W/R	FFWCTL30[7:0]							
#95	0x5F		W/R	FFWCTL31[7:0]							
#96	0x60		W/R	FFWCTL32[7:0]							
#97	0x61		W/R	FFWCTL33[7:0]							
#98	0x62		W/R	FFWCTL34[7:0]							
#99	0x63		W/R	FFWCTL35[7:0]							
#100	0x64		W/R	FFWCTL36[7:0]							
#101	0x65		W/R	FFWCTL37[7:0]							
#102	0x66		W/R	FFWCTL38[7:0]							
#103	0x67		W/R	FFWCTL39[7:0]							
#104	0x68		W/R	FFWCTL40[7:0]							
#105	0x69		W/R	FFWCTL41[7:0]							
#106	0x6A		W/R	FFWCTL42[7:0]							
#107	0x6B		W/R	FFWCTL43[7:0]							
#108	0x6C		W/R	FFWCTL44[7:0]							
#109	0x6D		W/R	FFWCTL45[7:0]							
#110	0x6E		W/R	FFWCTL46[7:0]							
#111	0x6F		W/R	FFWCTL47[7:0]							
#112	0x70		W/R	FFWCTL48[7:0]							
#113	0x71		W/R	FFWCTL49[7:0]							
#114	0x72		W/R	FFWCTL50[7:0]							
#115	0x73		W/R	FFWCTL51[7:0]							
#116	0x74		W/R	FFWCTL52[7:0]							
#117	0x75		W/R	FFWCTL53[7:0]							
#118	0x76		W/R	FFWCTL54[7:0]							
#119	0x77		W/R	FFWCTL55[7:0]							
#120	0x78		W/R	FFWCTL56[7:0]							
#121	0x79		W/R	FFWCTL57[7:0]							
#122	0x7A		W/R	FFWCTL58[7:0]							
#123	0x7B		W/R	FFWCTL59[7:0]							
#124	0x7C		W/R	FFWCTL60[7:0]							
#125	0x7D		W/R	FFWCTL61[7:0]							
#126	0x7E		W/R	FFWCTL62[7:0]							
#127	0x7F		W/R	FFWCTL63[7:0]							

7.3.9 ANA_REG (Analog volume, Mixer, etc.)

ANA_REG DEC	ANA_REG HEX	Function	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#0	0x00	Hardware ID	R	ANA_ID[7:0]							
#1	0x01	Reset	W/R	"0"	"0"	"0"	"0"	"0"	"0"	"0"	ANA_RST
#2	0x02	Power Management	W/R	"0"	"0"	"0"	AP_LDOA	AP_LDO12	"0"	"1"	AP_VR
#6	0x06		W/R	AP_MC4	AP_MC3	AP_MC2	AP_MC1	"0"	AP_MB3	AP_MB2	AP_MB1
#7	0x07		W/R	"0"	"0"	"0"	"0"	"0"	AP_ADM	AP_ADR	AP_ADL
#12	0x0C	Flag	R	LO2R_BUSY	LO2L_BUSY	LO1R_BUSY	LO1L_BUSY	"0"	"0"	"0"	"0"
#13	0x0D	Mic bias	W/R	"0"	"0"	MBSEL3[1:0]		MBSEL2[1:0]		MBSEL1[1:0]	
#14	0x0E	Power Control	W/R	"0"	MBS3_DISCH	MBS2_DISCH	MBS1_DISCH	"0"	"0"	"0"	"0"
#24	0x18	Pin Control	W/R	"0"	"0"	DIF_LO2	DIF_LO1	"0"	"0"	"0"	"0"
#27	0x1B	Volume	W/R	"0"	"0"	MC1VOL[5:0]					
#28	0x1C		W/R	"0"	"0"	MC2VOL[5:0]					
#29	0x1D		W/R	"0"	"0"	MC3VOL[5:0]					
#30	0x1E		W/R	"0"	"0"	MC4VOL[5:0]					
#36	0x24	Volume	W/R	ALAT_LO1	LO1VOL_L[6:0]						
#37	0x25		W/R	"0"	LO1VOL_R[6:0]						
#38	0x26		W/R	ALAT_LO2	LO2VOL_L[6:0]						
#39	0x27		W/R	"0"	LO2VOL_R[6:0]						
#41	0x29	Volume	W/R	"0"	"0"	"0"	SVOL_LO2	SVOL_LO1	"0"	"0"	"0"
#44	0x2C	Pin Control	W/R	MC4SNG	MC3SNG	MC2SNG	MC1SNG	"0"	"0"	"0"	"0"
#45	0x2D	Flag	R	"0"	VREF_RDY	"0"	"0"	"0"	"0"	"0"	"0"
#46	0x2E		R	LO2RDY_R	LO2RDY_L	LO1RDY_R	LO1RDY_L	"0"	"0"	"0"	"0"
#48	0x30	Analog Mixer	W/R	ADL_M4MIX	ADL_M3MIX	ADL_M2MIX	ADL_M1MIX	"0"	"0"	"0"	"0"
#49	0x31		W/R	ADR_M4MIX	ADR_M3MIX	ADR_M2MIX	ADR_M1MIX	"0"	"0"	"0"	"0"
#50	0x32		W/R	ADM_M4MIX	ADM_M3MIX	ADM_M2MIX	ADM_M1MIX	"0"	"0"	"0"	"0"
#51	0x33	Error Flag	R	"0"	"0"	"0"	"0"	"0"	"0"	"0"	OTP
#55	0x37	Power Management	W/R	AP_LDOCP	"1"	"0"	"0"	"0"	"0"	"0"	AP_ADX
#56	0x38	Analog Mixer	W/R	ADX_M4MIX	ADX_M3MIX	ADX_M2MIX	ADX_M1MIX	"0"	"0"	"0"	"0"
#57	0x39	Flag	R	LDOCP_RDY	LDO18_RDY	"0"	LDOA_RDY	LDO12_RDY	MBS3_RDY	MBS2_RDY	MBS1_RDY
#58	0x3A	LDOCP/Charge Pump	W/R	"0"	"0"	"0"	LDOCP_LIM_ON	"0"	"0"	"0"	"0"

7.3.10 CD_REG

CD_REG		Function	W/R	D7	D6	D5	D4	D3	D2	D1	D0
DEC	HEX										
#1	0x01	Reset	W/R	"0"	"0"	"0"	"0"	"0"	"0"	"0"	CD_RST
#2	0x02	Power Management	W/R	"0"	DP_ADC	DP_DAC1	DP_DAC0	"0"	DP_PDMCK	DP_PDMADC	DP_PDMDAC
#40	0x28	ADX	W/R	"0"	DP_ADCX	"0"	"0"	"0"	DP_ADCLK	DP_ADOUT	"0"
#41	0x29	SCP	W/R	"0"	"0"	"0"	"0"	"0"	"0"	"0"	DP_CLKI
#43	0x2B	GPIO	W/R	"0"	"0"	"0"	"0"	EIRQGPIO	"0"	"0"	"0"
#44	0x2C	GPIO	W/R	GP0_INTE	"0"	GP0_DDR	GP0_DATA	"0"	"0"	GP0_MSK	GP0_INV
#45	0x2D	GPIO	W/R	GP1_INTE	"0"	GP1_DDR	GP1_DATA	"0"	"0"	GP1_MSK	GP1_INV
#46	0x2E	GPIO	W/R	GP2_INTE	"0"	GP2_DDR	GP2_DATA	"0"	"0"	GP2_MSK	GP2_INV
#47	0x2F	GPIO	W/R	GP3_INTE	"0"	GP3_DDR	GP3_DATA	"0"	"0"	GP3_MSK	GP3_INV
#48	0x30	Offset Cancellation	W/R	"0"	"0"	"0"	"0"	EIRQOFC	"0"	"0"	"0"
#49	0x31		W/R	"0"	"0"	"0"	"0"	SOFFCANFIN	OFFCAN_BSY	"0"	"0"

7.4 IF_REG Details

7.4.1 Intermediate Register Access

Access to *Intermediate Registers* is provided by the *Interface Register*.

7.4.1.1 A_REG_AINC

IF_REG	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#0 (0x00)	W/R	A_REG_AINC	A_REG_A[6:0]						

<Description>
This register bit enables or disables auto A_REG_A register increment feature.
Enabling this bit ("1") increments the register address by 1 when data is written into A_REG_D (IF_REG#1) register, but does not when data is read from the A_REG_D register.
A_REG pointed to by this A_REG_A changes after every writes through A_REG_D when enabled.

<Reset Value>
"0"

<Reset Conditions>
1. At power on resets
2. When putting "1" in the software reset bit RST_A

<Access During Power Save State>
Allowed

7.4.1.2 A_REG_A

IF_REG	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#0 (0x00)	W/R	A_REG_AINC	A_REG_A[6:0]						

<Description>
This register specifies an *Intermediate Register* address (A_REG#).
This register value auto increments by 1 when data is written into the A_REG_D (IF_REG#1) register with A_REG_AINC = "1", but does not when data is read from the register.

<Reset Value>
"7'h00"

<Reset Conditions>
1. At power on resets
2. When putting "1" in the software reset bit RST_A

<Access During Power Save State>
Allowed

NOTICE

The register address returns to 0 when A_REG_A goes beyond "7'h7F" (#127) with A_REG_AINC = "1".

7.4.1.3 A_REG_D

IF_REG	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#1 (0x01)	W/R	A_REG_D[7:0]							

<Description>
This register specifies a value to be written into the *Intermediate Register* address specified with the A_REG_A (IF_REG#0) register during write access.
During reads, data is read from the address specified.

<Reset Value>
-

<Reset Conditions>
-

<Access During Power Save State>
The accessibility depends on an address specified with A_REG_A (IF_REG#0).
Registers inaccessible during power-saving mode cannot be written or may have invalid data.

7.4.1.4 E_REG_AINC

IF_REG	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#32 (0x20)	W/R	E_REG_AINC	E_REG_A[6:0]						

<Description>
This register bit enables or disables auto E_REG_A register increment feature.
Enabling this bit ("1") increments the register address by 1 when data is written into E_REG_D (IF_REG#33) register, but does not when data is read from the E_REG_D register.

<Reset Value>
"0"

<Reset Conditions>
1. At power on resets
2. When putting "1" in the software reset bit RST_A

<Access During Power Save State>
Allowed

7.4.1.5 E_REG_A

IF_REG	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#32 (0x20)	W/R	E_REG_AINC	E_REG_A[6:0]						

<Description>
This register bit specifies an *Intermediate Register* number (E_REG#).
This register value auto increments by 1 when data is written into E_REG_D (IF_REG#33) register with E_REG_AINC = "1", but does not when data is read from the E_REG_D register.

<Reset Value>
"7'h00"

<Reset Conditions>
1. At power on resets
2. When putting "1" in the software reset bit RST_A

<Access During Power Save State>
Allowed

NOTICE

The register address returns to 0 when E_REG_A goes beyond "7'h7F" (#127) with E_REG_AINC = "1".

7.4.1.6 E_REG_D

IF_REG	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#33 (0x21)	W/R	E_REG_D[7:0]							

<Description>
This register specifies a value to be written into an *Intermediate Register* address specified with the E_REG_A (IF_REG#32) register during write access.
During reads, data is read from the address specified.

<Reset Value>
-

<Reset Conditions>
-

<Access During Power Save State>
The accessibility depends on an address specified with E_REG_A (IF_REG#32).
Registers inaccessible during power-saving mode cannot be written or may have invalid data.

7.4.1.7 ANA_REG_AINC

IF_REG	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#6 (0x06)	W/R	ANA_REG_AINC	ANA_REG_A[6:0]						

<Description>
This register bit enables or disables auto ANA_REG_A register increment feature.
Enabling this bit ("1") increments the register address by 1 when data is written into ANA_REG_D (IF_REG#7) register, but does not when data is read from the register.

<Reset Value>
"0"

<Reset Conditions>
At power on resets

<Access During Power Save State>
Allowed

7.4.1.8 ANA_REG_A

IF_REG	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#6 (0x06)	W/R	ANA_REG_AINC	ANA_REG_A[6:0]						

<Description>
This register specifies an *Intermediate Register* address (ANA_REG#).
This register value auto increments by 1 when data is written into ANA_REG_D (IF_REG#7) register with ANA_REG_AINC = "1", but does not when data is read from the register.

<Reset Value>
"7'h00"

<Reset Conditions>
At power on resets

<Access During Power Save State>
Allowed

NOTICE

The register address returns to 0 when ANA_REG_A goes beyond "7'h7F" (#127) with ANA_REG_AINC set to "1".

7.4.1.9 ANA_REG_D

IF_REG	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#7 (0x07)	W/R	ANA_REG_D[7:0]							

<Description>
This register specifies a value to be written into an *Intermediate Register* address specified with the ANA_REG_A (IF_REG#6) register during write access.
During reads, data is read from the address specified.

<Reset Value>
-

<Reset Conditions>
-

<Access During Power Save State>
The accessibility depends on an address specified with ANA_REG_A (IF_REG#6).
Registers inaccessible during power-saving mode cannot be written or may have invalid data.

7.4.1.10 CD_REG_AINC

IF_REG	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#8 (0x08)	W/R	CD_REG_AINC	CD_REG_A[6:0]						

<Description>
This register bit enables or disables auto CD_REG_A register increment feature.
Enabling this bit ("1") increments the register address by 1 when data is written into the CD_REG_D (IF_REG#9) register, but does not when data is read from the register.

<Reset Value>
"0"

<Reset Conditions>
At power on resets

<Access During Power Save State>
Allowed

7.4.1.11 CD_REG_A

IF_REG	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#8 (0x08)	W/R	CD_REG_AINC	CD_REG_A[6:0]						

<Description>
This register specifies an *Intermediate Register* address (CD_REG#).
This register value auto increments by 1 when data is written into the CD_REG_D (IF_REG#9) register with CD_REG_AINC = "1", but does not when data is read from the register.

<Reset Value>
"7'h00"

<Reset Conditions>
At power on resets

<Access During Power Save State>
Allowed

NOTICE

The register address returns to 0 when CD_REG_A goes beyond "7'h7F" (#127) with CD_REG_AINC set to "1".

7.4.1.12 CD_REG_D

IF_REG	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#9 (0x09)	W/R	CD_REG_D[7:0]							

<Description>
This register specifies a value to be written into an *Intermediate Register* address specified with CD_REG_A (IF_REG#8) register during write access.
During reads, data is read from the address specified.

<Reset Value>
-

<Reset Conditions>
-

<Access During Power Save State>
The accessibility depends on an address specified with CD_REG_A (IF_REG#8).
Registers inaccessible during power-saving mode cannot be written or may have invalid data.

7.4.2 Power Management

7.4.2.1 PSW_[M/F/C]_OFF

IF_REG	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#3 (0x03)	W	"1"	PSW_M_OFF	PSW_F_OFF	PSW_C_OFF	"1"	RST_M	RST_F	RST_C

<Description>

This bit controls its corresponding power switch in the power domain [M/F/C].

"0": Power supply ON

"1": Power supply OFF (default)

<Reset Value>

"1"

<Reset Conditions>

1. At power on resets
2. When putting "1" in the software reset bit RST_A

<Access During Power Save State>

Allowed

NOTICE

Do not power off while RST_[M/F/C] bit is "0", or leakage current may continue to flow.

7.4.2.2 PSW_[M/F/C]_FLAG

IF_REG	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#3 (0x03)	R	"1"	PSW_M_FLAG	PSW_F_FLAG	PSW_C_FLAG	"1"	RST_M	RST_F	RST_C

<Description>

This register bit indicates the current power status of whether the power supply has been supplied.

"0": Power being supplied

"1": Power not supplied.

Times below shows the latency from when PSW_[M/F/C]_OFF is written until its corresponding flag is set to either level.

PSW_M_FLAG : Approx. 1.5 µs
PSW_F_FLAG : Approx. 1.5 µs
PSW_C_FLAG : Approx. 2.0 µs

<Reset Value>

"1"

<Reset Conditions>

1. At power on resets
2. When putting "1" in the software reset bit RST_A

<Access During Power Save State>

Allowed

7.4.3 Reset

7.4.3.1 RST_A

IF_REG	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#2 (0x02)	W/R	"0"	"0"	"0"	"0"	"0"	"0"	"0"	RST_A

<Description>
Writing "1" to this bit resets the entire *1.2V digital block*.
"0": Reset disabled (Write), Not in reset state (Read)
"1": Reset enabled (Write), Reset state (Read)

<Reset Value>
"1"

<Reset Conditions>
At power on resets

<Access During Power Save State>
Allowed

7.4.3.2 RST_[M/F/C]

IF_REG	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#3 (0x03)	W	"1"	PSW_M_OFF	PSW_F_OFF	PSW_C_OFF	"1"	RST_M	RST_F	RST_C

<Description>
This register bit controls the software reset of its corresponding power domain [M/F/C].
"0": Software reset disabled
"1": Software reset state (default)

<Reset Value>
"1"

<Reset Conditions>
1. At power on resets
2. When putting "1" in the software reset bit RST_A

<Access During Power Save State>
Allowed

NOTICE

Do not set to "0" while "0" is read from PSW_[M/F/C]_OFF_FLAG (IF_REG#2), or leakage current may continue to flow.

7.5 A_REG Details

7.5.1 DevID / VerID

A_REG	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#0 (0x00)	R	DevID					VerID		

<Description>
These are two register fields, one for device ID and the other for chip revisions. Read only.

<Reset Value>
DevID: "5'b10001"
VerID: "3'b001"

<Reset Conditions>
-

<Access During Power Save State>
Allowed

7.5.2 CLOCK

7.5.2.1 PLL_PD

A_REG	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#2 (0x02)	W/R	PLL_PD	ANACLK_PD	PE_CLK_PD	PB_CLK_PD	PM_CLK_PD	PF_CLK_PD	PC_CLK_PD	VCOOUT_PD

<Description>
This register bit controls PLL power-saving mode.
"0": power-saving mode not activated
"1": power-saving mode activated (default)

<Reset Value>
"1"

<Reset Conditions>
1. At power on resets
2. When putting "1" in the software reset bit RST_A

<Access During Power Save State>
Allowed

7.5.2.2 [ANA/PE_/PB_/PM_/PF_/PC_]CLK_PD

A_REG	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#2 (0x02)	W/R	PLL_PD	ANACLK_PD	PE_CLK_PD	PB_CLK_PD	PM_CLK_PD	PF_CLK_PD	PC_CLK_PD	VCOOUT_PD

<Description>

This register bit controls the activation of clocks.

ANACLK_PD: clock for analog block
PE_CLK_PD: clock for E-DSP; Set this bit to "0" to use mixers.
PB_CLK_PD: clock for B-DSP
PM_CLK_PD: clock for mixers, SRC
PF_CLK_PD: clock for F-DSP
PC_CLK_PD: clock for C-DSP

To run clocks, unmask VCOOUT_PD in advance.

"0": Clock running (unmasked)
"1": Clock stopped (default)

<Reset Value>

All "1"

<Reset Conditions>

1. At power on resets
2. When putting "1" in the software reset bit RST_A

<Access During Power Save State>

Allowed

7.5.2.3 VCOOUT_PD

A_REG	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#2 (0x02)	W/R	PLL_PD	"0"	PE_CLK_PD	PB_CLK_PD	PM_CLK_PD	PF_CLK_PD	PC_CLK_PD	VCOOUT_PD

<Description>

This register bit will mask the PLL output.
To unmask the output, do it after the PLL is stabilized.

"0": Clock operating (unmasked)
"1": Clock stopped (default)

<Reset Value>

All "1"

<Reset Conditions>

1. At power on resets
2. When putting "1" in the software reset bit RST_A

<Access During Power Save State>

Allowed

7.5.3 Digital Interface Pin Controls

7.5.3.1 DO[1/2]_DRV

A_REG	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#5 (0x05)	W/R	DO1 _DRV	BCLK1 _INV	BCLK1 _MSK	BCLK1 _DDR	LRCK1 _MSK	LRCK1 _DDR	SDIN1 _MSK	SDO1 _DDR
#6 (0x06)	W/R	DO2 _DRV	BCLK2 _INV	BCLK2 _MSK	BCLK2 _DDR	LRCK2 _MSK	LRCK2 _DDR	SDIN2 _MSK	SDO2 _DDR

<Description>

This register bit specifies the current driving capability of BCLK[1/2] (output), LRCK[1/2] (output), and SDOUT[1/2] pin output driver.

DO1_DRV: Audio interface#1 (BCLK1, LRCK1, SDOUT1)

DO2_DRV: Audio interface#2 (BCLK2, LRCK2, SDOUT2)

When I/O supply (IOVDD[1/2]) is lower than 2.5 V, you can use the high current setting. Use the low current setting for 2.5 V or higher supply to reduce power consumption and also prevent overshoots and undershoots.

"0": Low current driving capability

"1": High current driving capability

<Reset Value>

All "0"

<Reset Conditions>

1. At power on resets
2. When putting "1" in the software reset bit RST_A

<Access During Power Save State>

Allowed

7.5.3.2 BCLK[1/2]_INV

A_REG	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#5 (0x05)	W/R	DO1_DRV	BCLK1_INV	BCLK1_MSK	BCLK1_DDR	LRCK1_MSK	LRCK1_DDR	SDIN1_MSK	SDO1_DDR
#6 (0x06)	W/R	DO2_DRV	BCLK2_INV	BCLK2_MSK	BCLK2_DDR	LRCK2_MSK	LRCK2_DDR	SDIN2_MSK	SDO2_DDR

<Description>

This register bit specifies the polarity of BCLK[1/2] in digital audio interface operation.

"0": Normal operation

"1": Polarity reversed

<Reset Value>

All "0"

<Reset Conditions>

1. At power on resets
2. When putting "1" in the software reset bit RST_A

<Access During Power Save State>

Allowed

7.5.3.3 [BCLK/LRCK/SDIN][1/2]_MSK

A_REG	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#5 (0x05)	W/R	DO1_DRV	BCLK1_INV	BCLK1_MSK	BCLK1_DDR	LRCK1_MSK	LRCK1_DDR	SDIN1_MSK	SDO1_DDR
#6 (0x06)	W/R	DO2_DRV	BCLK2_INV	BCLK2_MSK	BCLK2_DDR	LRCK2_MSK	LRCK2_DDR	SDIN2_MSK	SDO2_DDR

<Description>

These register bits are used to mask or unmask BCLK[1/2], LRCK[1/2], and SDIN[1/2] input pins.

"0": Unmasked

"1": Masked

<Reset Value>

All "1"

<Reset Conditions>

1. At power on resets
2. When putting "1" in the software reset bit RST_A

<Access During Power Save State>

Allowed

7.5.3.4 [BCLK/LRCK/SDO][1/2]_DDR

A_REG	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#5 (0x05)	W/R	DO1_DRV	BCLK1_INV	BCLK1_MSK	BCLK1_DDR	LRCK1_MSK	LRCK1_DDR	SDIN1_MSK	SDO1_DDR
#6 (0x06)	W/R	DO2_DRV	BCLK2_INV	BCLK2_MSK	BCLK2_DDR	LRCK2_MSK	LRCK2_DDR	SDIN2_MSK	SDO2_DDR

<Description>
These register bits control the input and output direction for BCLK[1/2], LRCK[1/2], and SDOOUT[1/2] pins.
"0": Input
"1": Output

<Reset Value>
All "0"

<Reset Conditions>
1. At power on resets
2. When putting "1" in the software reset bit RST_A

<Access During Power Save State>
Allowed

7.5.3.5 PDM[0/1]_DATA_DELAY

A_REG	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#8 (0x08)	W/R	"0"	"0"	PDM1_DATA_DELAY	PDM0_DATA_DELAY	"0"	PCMOUT2_HIZ	PCMOUT1_HIZ	"0"

<Description>
This register bit specifies whether to delay DMDIN[0/1] signal by approx. 10 ns relative to DMCK or not. Depending on the digital microphone used, set this bit to "1" when you need to hold the signals.
"0": Delay disabled
"1": Delay enabled

<Reset Value>
All "0"

<Reset Conditions>
1. At power on resets
2. When putting "1" in the software reset bit RST_A

<Access During Power Save State>
Allowed

7.5.3.6 PCMOUT[1/2]_HIZ

A_REG	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#8 (0x08)	W/R	"0"	"0"	PDM1_DATA_DELAY	PDM0_DATA_DELAY	"0"	PCMOUT2_HIZ	PCMOUT1_HIZ	"0"

<Description>

This register bit selects a logic state to be held at SDOUT[1/2] pin while no data is being transmitted in PCM interface mode.

In digital audio I/F mode, these settings are ignored and the output pin is always held low.

"0": "L" level output (default)

"1": High-impedance state

<Reset Value>

All "0"

<Reset Conditions>

1. At power on resets
2. When putting "1" in the software reset bit RST_A

<Access During Power Save State>

Allowed

7.5.4 GPIO (PA[0/1/2]) Pin Controls

The table below shows the relationship between digital microphone interface pins and control registers.

Pin Name	Register
DMCK	PA0
DMDIN0	PA1
DMDIN1	PA2

7.5.4.1 PA0_OUT, PA[0/1/2]_DDR

A_REG	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#9 (0x09)	W/R	PA0_OUT	"0"	PA0_DDR	PA0_DATA	"0"	PA0_OUTSEL	PA0_MSK	PA0_INV
#10 (0x0A)	W/R	"0"	"0"	PA1_DDR	PA1_DATA	"0"	PA1_OUTSEL	PA1_MSK	PA1_INV
#11 (0x0B)	W/R	"0"	"0"	PA2_DDR	PA2_DATA	"0"	PA2_OUTSEL	PA2_MSK	PA2_INV

<Description>
These registers must be configured appropriately when the digital microphone interface is used: PA0_OUT = PA0_DDR = "1", PA[1/2]_DDR = " 0".

<Reset Value>
All "0"

<Reset Conditions>
1. At power on resets
2. When putting "1" in the software reset bit RST_A

<Access During Power Save State>
Allowed

7.5.4.2 PA[0/1/2]_DATA

A_REG	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#9 (0x09)	W/R	PA0_OUT	"0"	PA0_DDR	PA0_DATA	"0"	PA0_OUTSEL	PA0_MSK	PA0_INV
#10 (0x0A)	W/R	"0"	"0"	PA1_DDR	PA1_DATA	"0"	PA1_OUTSEL	PA1_MSK	PA1_INV
#11 (0x0B)	W/R	"0"	"0"	PA2_DDR	PA2_DATA	"0"	PA2_OUTSEL	PA2_MSK	PA2_INV

<Description>
These registers need not to be changed from initial values when the digital microphone interface is used.

<Reset Value>
All "0"

<Reset Conditions>
1. At power on resets
2. When putting "1" in the software reset bit RST_A

<Access During Power Save State>
Allowed

7.5.4.3 PA[0/1/2]_OUTSEL

A_REG	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#9 (0x09)	W/R	PA0_ OUT	"0"	PA0_ DDR	PA0_ DATA	"0"	PA0_ OUTSEL	PA0_ MSK	PA0_ INV
#10 (0x0A)	W/R	"0"	"0"	PA1_ DDR	PA1_ DATA	"0"	PA1_ OUTSEL	PA1_ MSK	PA1_ INV
#11 (0x0B)	W/R	"0"	"0"	PA2_ DDR	PA2_ DATA	"0"	PA2_ OUTSEL	PA2_ MSK	PA2_ INV

<Description>
These registers need not to be changed from initial values when the digital microphone interface is used.

<Reset Value>
All "0"

<Reset Conditions>
1. At power on resets
2. When putting "1" in the software reset bit RST_A

<Access During Power Save State>
Allowed

7.5.4.4 PA[0/1/2]_MSK

A_REG	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#9 (0x09)	W/R	PA0_ OUT	"0"	PA0_ DDR	PA0_ DATA	"0"	PA0_ OUTSEL	PA0_ MSK	PA0_ INV
#10 (0x0A)	W/R	"0"	"0"	PA1_ DDR	PA1_ DATA	"0"	PA1_ OUTSEL	PA1_ MSK	PA1_ INV
#11 (0x0B)	W/R	"0"	"0"	PA2_ DDR	PA2_ DATA	"0"	PA2_ OUTSEL	PA2_ MSK	PA2_ INV

<Description>
These registers must be configured appropriately when the digital microphone interface is used: PA0_MSK = "1", PA[1/2]_MSK = " 0".

<Reset Value>
"1"

<Reset Conditions>
1. At power on resets
2. When putting "1" in the software reset bit RST_A

<Access During Power Save State>
Allowed

7.5.4.5 PA[0/1/2]_INV

A_REG	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#9 (0x09)	W/R	PA0_OUT	"0"	PA0_DDR	PA0_DATA	"0"	PA0_OUTSEL	PA0_MSK	PA0_INV
#10 (0x0A)	W/R	"0"	"0"	PA1_DDR	PA1_DATA	"0"	PA1_OUTSEL	PA1_MSK	PA1_INV
#11 (0x0B)	W/R	"0"	"0"	PA2_DDR	PA2_DATA	"0"	PA2_OUTSEL	PA2_MSK	PA2_INV

<Description>
These registers need not to be changed from initial values when the digital microphone interface is used.

<Reset Value>
All "0"

<Reset Conditions>
1. At power on resets
2. When putting "1" in the software reset bit RST_A

<Access During Power Save State>
Allowed

7.5.5 PLL / Clock

PLL supports a reference frequency ranging from 2 MHz to 27 MHz; however, CLKI must be 24.576 MHz when the device is used in SPI master mode.

7.5.5.1 PLL Block Diagram

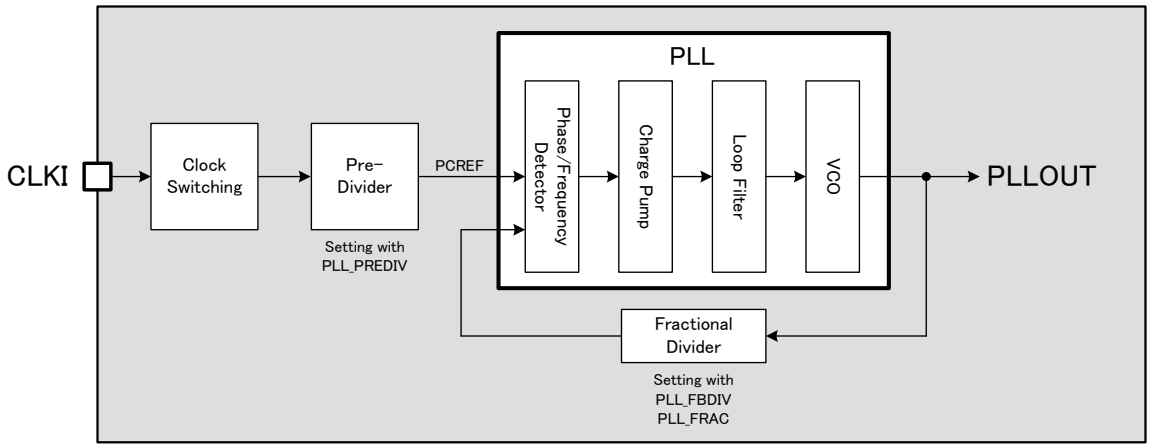


Figure 7-2. PLL block diagram.

7.5.5.2 PLL Output Frequency

PLL output frequency f_{VCOCK} [MHz] can be determined as follows.

$$f_{PCREF} = \frac{f_{CLKI}}{PLL\_PREDIV}$$

$$f_{VCOCK} = f_{PCREF} \times (PLL\_FBDIV + \frac{PLL\_FRAC}{65536})$$

PLL_PREDIV must be configured so that f_{PCREF} becomes within the range of 1 MHz to 2 MHz.

The tables below show the PLL register setting values for each typical clock input frequency.

Table 7.2. PLL register settings for outputting 147.456 MHz

Clock Input Frequency [Hz]	PLL_ PS	PLL_ INT	PLL_ PREDIV	PLL_ FBDIV	PLL_ FRAC	PLL_ FOUT	PLL Output Frequency [MHz]
2M	0	0	1	73	47710	1	147.45599365
12M	1	0	11	135	11010	1	147.45599920
12.288M	1	1	7	84	0	1	147.45600000
24M	1	0	22	135	11010	1	147.45599920
24.576M	1	1	13	78	0	1	147.45600000
26M	1	0	22	124	50493	1	147.45600059

Table 7.3. PLL register settings for outputting 73.728 MHz

Clock Input Frequency [Hz]	PLL_ PS	PLL_ INT	PLL_ PREDIV	PLL_ FBDIV	PLL_ FRAC	PLL_ FOUT	PLL Output Frequency [MHz]
2M	0	0	1	36	56623	0	73.72799683
12M	1	0	11	67	38273	0	73.72799960
12.288M	1	1	7	42	0	0	73.72800000
24M	1	0	22	67	38273	0	73.72799960
24.576M	1	1	13	39	0	0	73.72800000
26M	1	0	15	42	35087	0	73.72800090

7.5.5.3 PLL_PS

A_REG	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#24 (0x18)	W/R	"0"	"0"	"0"	"0"	"0"	PLL_PS	"0"	PLL_INT

<Description>
This register bit controls PLL prescaler (R divider).
When this bit is set to"0", set its corresponding PLL_PREDIV bit to "1" to calculate the PLL output frequency.
Set this PLL_PS bit to "0" in LOWFIN mode.
"0": Prescaler not used
"1": Prescaler used (default)

<Reset Value>
"1"

<Reset Conditions>
1. At power on resets
2. When putting "1" in the software reset bit RST_A

<Access During Power Save State>
Allowed

7.5.5.4 PLL_INT

A_REG	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#24 (0x18)	W/R	"0"	"0"	"0"	"0"	"0"	PLL_PS	"0"	PLL_INT

<Description>
Set this bit to "1" when the PLL output clock frequency is an integral multiple of its input clock.
Use PLL_FRAC = "0" when PLL_INT bit is "1" to calculate the PLL output frequency.
"0": Not in an integral multiple relation (default)
"1": In an integral multiple relation

<Reset Value>
"0"

<Reset Conditions>
1. At power on resets
2. When putting "1" in the software reset bit RST_A

<Access During Power Save State>
Allowed

7.5.5.5 PLL_PREDIV

A_REG	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#25 (0x19)	W/R	"0"	"0"	PLL_PREDIV[5:0]					

<Description>
This register specifies the f_{PCREF} clock division factor to the PLL input clock.
Do not set this register to "1" when the PLL_PS is set to "1".

<Reset Value>
"6'h00"

<Reset Conditions>
1. At power on resets
2. When putting "1" in the software reset bit RST_A

<Access During Power Save State>
Allowed

7.5.5.6 PLL_FBDIV

A_REG	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#26 (0x1A)	W/R	"0"	"0"	PLL_FBDIV[13:8]					
#27 (0x1B)	W/R	PLL_FBDIV[7:0]							

<Description>
These registers specify divider (integral part) values on the feedback path.
See *7.5.6 Clock Settings* for the calculation formula.
Do not set this register to "1".
Do not set to "2" when you calculate Fraction (PLL0_INT = "0").

<Reset Value>
"14'h0000"

<Reset Conditions>
1. At power on resets
2. When putting "1" in the software reset bit RST_A

<Access During Power Save State>
Allowed

7.5.5.7 PLL_FRAC

A_REG	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#28 (0x1C)	W/R	PLL_FRAC[15:8]							
#29 (0x1D)	W/R	PLL_FRAC[7:0]							

<Description>
These registers specify divider (fractional part) values on the feedback path.
See *7.5.6 Clock Settings* for the calculation formula.

<Reset Value>
"16'h0000"

<Reset Conditions>
1. At power on resets
2. When putting "1" in the software reset bit RST_A

<Access During Power Save State>
Allowed

7.5.5.8 PLL_FOUT

A_REG	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#30(0x1E)	W/R	"0"	"0"	"0"	"0"	"0"	"0"	PLL_FOUT	"0"

<Description>
This register bit selects a PLL output frequency of 73.728 MHz or 147.456 MHz.
Set this bit to "1" when F-DSP (FDSP_DIVR in A_REG#19) and C-DSP (CDSP_DIVR) operation frequencies are generated from 147.456 MHz, and to "0" when they are generated from 73.728MHz.
"0": 73.728 MHz (default)
"1": 147.456 MHz

<Reset Value>
"6'h00"

<Reset Conditions>
1. At power on resets
2. When putting "1" in the software reset bit RST_A

<Access During Power Save State>
Allowed

7.5.6 Clock Settings

7.5.6.1 FDSP_DIVR

A_REG	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#19 (0x13)	W/R	FDSP_DIVR[1:0]		"0"	FREQ73M	"0"	CDSP_DIVR[2:0]		

<Description>

FDSP_DIVR register specifies F−DSP clock frequency as a fraction of the PLL output frequency. F−DSP must be in *Power Save State* when changing this register.

Table 7.4. F-DSP clock frequency

FDSP_DIVR	F-DSP clock frequency	
	When PLL output is 147.456 MHz	When PLL output is 73.728MHz
"0": 1/1	147.456 MHz	73.728 MHz
"1": 1/2	73.728 MHz	36.864 MHz
"2": 1/3	49.152 MHz	24.576 MHz
"3": 1/4	36.864 MHz	18.432 MHz

<Reset Value>

"2'b00"

<Reset Conditions>

1. On power−on resets
2. When putting "1" in the software reset bit RST_A

<Access During Power Save State>

Allowed

7.5.6.2 FREQ73M

A_REG	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#19 (0x13)	W/R	FDSP_DIVR[1:0]		"0"	FREQ73M	"0"	CDSP_DIVR[2:0]		

<Description>

FREQ73M register must be set to a value which matches the PLL output frequency.

Mixer, SRC, B−DSP, and *E−DSP* block runs on a clock frequency determined by this value.

"0": when PLL output is 73.728MHz

"1": when PLL output is 147.456MHz

<Reset Value>

"0"

<Reset Conditions>

1. On power−on resets
2. When putting "1" in the software reset bit RST_A

<Access During Power Save State>

Allowed

7.5.6.3 CDSP_DIVR

A_REG	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#19 (0x13)	W/R	FDSP_DIVR[1:0]		"0"	FREQ73M	"0"	CDSP_DIVR[2:0]		

<Description>

CDSP_DIVR register specifies C−DSP clock frequency as a fraction of the PLL output frequency. C−DSP must be in *Power Save State* when changing this register.

Table 7.5. C-DSP clock frequency

CDSP_DIVR	C-DSP clock frequency	
	When PLL output is 147.456 MHz	When PLL output is 73.728 MHz
"0": 1/1	147.456 MHz	73.728 MHz
"1": 1/2	73.728 MHz	36.864 MHz
"2": 1/3	49.152 MHz	24.576 MHz
"3": 1/4	36.864 MHz	18.432 MHz
"4": 1/6	24.576 MHz	12.288 MHz
"5": 1/8	18.432 MHz	9.216 MHz
"6": 1/16	9.216 MHz	–
"7": Reserved	–	–

<Reset Value>

"3'b000"

<Reset Conditions>

1. On power−on resets
2. When putting "1" in the software reset bit RST_A

<Access During Power Save State>

Allowed

7.6 MA_REG Details

7.6.1 Volume

7.6.1.1 ADI[0/1/2]_VINTP

MA_REG	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#4 (0x04)	W/R	"0"	ADI2_ VINTP	ADI1_ VINTP	ADI0_ VINTP	DIFI3_ VINTP	DIFI2_ VINTP	DIFI1_ VINTP	DIFI0_ VINTP

<Description>

ADI[0/1/2]_VINTP registers enable and disable hardware volume change smoothing for each of analog input ports, and volume changes with *ADI[0/1/2]_VOL[0/1]* are made smooth with a time constant of 20 ms. Putting "0" in these registers disable the smoothing.

"0": Disable volume change smoothing
"1": Enable volume change smoothing (default)

<Reset Value>

All "1"

<Reset Conditions>

1. On power−on resets
2. When putting "1" in the software reset bit RST_A
3. When putting "1" in the software reset bit RST_M

<Access During Power Save State>

Not allowed

7.6.1.2 DIFI[0/1/2/3]_VINTP

MA_REG	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#4 (0x04)	W/R	"0"	ADI2_ VINTP	ADI1_ VINTP	ADI0_ VINTP	DIFI3_ VINTP	DIFI2_ VINTP	DIFI1_ VINTP	DIFI0_ VINTP

<Description>

DIFI[0/1/2/3]_VINTP registers enable and disable hardware volume change smoothing for each of digital input ports, and volume changes with *DIFI[0/1/2/3]_VOL[0/1]* are made smooth with a time constant of 20 ms. Putting "0" in these registers disable the smoothing.

"0": Disable volume change smoothing
"1": Enable volume change smoothing (default)

<Reset Value>

All "1"

<Reset Conditions>

1. On power−on resets
2. When putting "1" in the software reset bit RST_A
3. When putting "1" in the software reset bit RST_M

<Access During Power Save State>

Not allowed

7.6.1.3 DAO[0/1]_VINTP

MA_REG	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#5 (0x05)	W/R	"0"	"0"	DAO1_ VINTP	DAO0_ VINTP	DIFO3_ VINTP	DIFO2_ VINTP	DIFO1_ VINTP	DIFO0_ VINTP

<Description>

DAO[0/1]_VINTP registers enable and disable hardware volume change smoothing for each port of analog output, and volume changes with *DAO[0/1]_VOL[0/1]* are made smooth with a time constant of 20 ms. Putting "0" in these registers disable the smoothing.

"0": Disable volume change smoothing
"1": Enable volume change smoothing (default)

<Reset Value>

All "1"

<Reset Conditions>

1. On power−on resets
2. When putting "1" in the software reset bit RST_A
3. When putting "1" in the software reset bit RST_M

<Access During Power Save State>

Not allowed

7.6.1.4 DIFO[0/1/2/3]_VINTP

MA_REG	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#5 (0x05)	W/R	"0"	"0"	DAO1_ VINTP	DAO0_ VINTP	DIFO3_ VINTP	DIFO2_ VINTP	DIFO1_ VINTP	DIFO0_ VINTP

<Description>

DIFO[0/1/2]_VINTP registers enable and disable hardware volume change smoothing for each of digital output ports, and volume changes with *DIFO[0/1/2]_VOL[0/1]* are made smooth with a time constant of 20 ms. Putting "0" in these registers disable the smoothing.

"0": Disable volume change smoothing
"1": Enable volume change smoothing (default)

<Reset Value>

All "1"

<Reset Conditions>

1. On power−on resets
2. When putting "1" in the software reset bit RST_A
3. When putting "1" in the software reset bit RST_M

<Access During Power Save State>

Not allowed

7.6.1.5 DIFI[0/1/2/3]_VSEP

MA_REG	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#6 (0x06)	W	DIFI0_VSEP	DIFI0_VOL0[6:0]						
#8 (0x08)	W	DIFI1_VSEP	DIFI1_VOL0[6:0]						
#10 (0x0A)	W	DIFI2_VSEP	DIFI2_VOL0[6:0]						
#12 (0x0C)	W	DIFI3_VSEP	DIFI3_VOL0[6:0]						

<Description>

Use this write-only register bit DIFI*m*_VSEP for each of ports [0/1/2/3] to control how input volume level change tracks each other. The *m* in DIFI*m*_VSEP maps to the logical port number #0 through #3.

"0": Writing in DIFI[0/1/2/3]_VOL*0* to change volume level makes DIFI[0/1/2/3]_VOL*1* level changed to the same level.
Writing in DIFI[0/1/2/3]_VOL*1* just changes DIFI[0/1/2/3]_VOL*1* level. (Default)

"1": Writing in DIFI[0/1/2/3]_VOL*1* to change volume level makes DIFI[0/1/2/3]_VOL*0* level changed to the same level.
Writing in DIFI[0/1/2/3]_VOL*0* just changes DIFI[0/1/2/3]_VOL*0* level.

<Reset Value>

All "0"

<Reset Conditions>

1. At power on resets
2. When putting "1" in the software reset bit RST_A
3. When putting "1" in the software reset bit RST_M

<Access During Power Save State>

Not allowed

7.6.1.6 DIFI[0/1/2/3]_VOL[0/1]

MA_REG	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#6 (0x06)	W/R	DIFI0_VSEP	DIFI0_VOL0[6:0]						
#7 (0x07)	W/R	"0"	DIFI0_VOL1[6:0]						
#8 (0x08)	W/R	DIFI1_VSEP	DIFI1_VOL0[6:0]						
#9 (0x09)	W/R	"0"	DIFI1_VOL1[6:0]						
#10 (0x0A)	W/R	DIFI2_VSEP	DIFI2_VOL0[6:0]						
#11 (0x0B)	W/R	"0"	DIFI2_VOL1[6:0]						
#12 (0x0C)	W/R	DIFI3_VSEP	DIFI3_VOL0[6:0]						
#13 (0x0D)	W/R	"0"	DIFI3_VOL1[6:0]						

<Description>

Use these registers to set digital audio input #[0/1/2/3] volume levels.

Adjust this register value as input source level changes.

"7'h00": Mute the input

"7'h01" through "7'h72": Attenuate or boost −95 dB through +18 dB in 1 dB step

"7'h72" to "7'h7F": Boost +18 dB

Table 7.6. Digital Audio Input Gain setting

Setting value		Volume	Setting value		Volume	Setting value		Volume	Setting value		Volume
DEC	HEX	Gain[dB]	DEC	HEX	Gain[dB]	DEC	HEX	Gain[dB]	DEC	HEX	Gain[dB]
0	7'h00	MUTE	32	7'h20	−64	64	7'h40	−32	96	7'h60	0
1	7'h01	−95	33	7'h21	−63	65	7'h41	−31	97	7'h61	1
2	7'h02	−94	34	7'h22	−62	66	7'h42	−30	98	7'h62	2
3	7'h03	−93	35	7'h23	−61	67	7'h43	−29	99	7'h63	3
4	7'h04	−92	36	7'h24	−60	68	7'h44	−28	100	7'h64	4
5	7'h05	−91	37	7'h25	−59	69	7'h45	−27	101	7'h65	5
6	7'h06	−90	38	7'h26	−58	70	7'h46	−26	102	7'h66	6
7	7'h07	−89	39	7'h27	−57	71	7'h47	−25	103	7'h67	7
8	7'h08	−88	40	7'h28	−56	72	7'h48	−24	104	7'h68	8
9	7'h09	−87	41	7'h29	−55	73	7'h49	−23	105	7'h69	9
10	7'h0A	−86	42	7'h2A	−54	74	7'h4A	−22	106	7'h6A	10
11	7'h0B	−85	43	7'h2B	−53	75	7'h4B	−21	107	7'h6B	11
12	7'h0C	−84	44	7'h2C	−52	76	7'h4C	−20	108	7'h6C	12
13	7'h0D	−83	45	7'h2D	−51	77	7'h4D	−19	109	7'h6D	13
14	7'h0E	−82	46	7'h2E	−50	78	7'h4E	−18	110	7'h6E	14
15	7'h0F	−81	47	7'h2F	−49	79	7'h4F	−17	111	7'h6F	15
16	7'h10	−80	48	7'h30	−48	80	7'h50	−16	112	7'h70	16
17	7'h11	−79	49	7'h31	−47	81	7'h51	−15	113	7'h71	17
18	7'h12	−78	50	7'h32	−46	82	7'h52	−14	114	7'h72	18
19	7'h13	−77	51	7'h33	−45	83	7'h53	−13	115	7'h73	18
20	7'h14	−76	52	7'h34	−44	84	7'h54	−12	116	7'h74	18
21	7'h15	−75	53	7'h35	−43	85	7'h55	−11	117	7'h75	18
22	7'h16	−74	54	7'h36	−42	86	7'h56	−10	118	7'h76	18
23	7'h17	−73	55	7'h37	−41	87	7'h57	−9	119	7'h77	18
24	7'h18	−72	56	7'h38	−40	88	7'h58	−8	120	7'h78	18
25	7'h19	−71	57	7'h39	−39	89	7'h59	−7	121	7'h79	18
26	7'h1A	−70	58	7'h3A	−38	90	7'h5A	−6	122	7'h7A	18
27	7'h1B	−69	59	7'h3B	−37	91	7'h5B	−5	123	7'h7B	18
28	7'h1C	−68	60	7'h3C	−36	92	7'h5C	−4	124	7'h7C	18
29	7'h1D	−67	61	7'h3D	−35	93	7'h5D	−3	125	7'h7D	18
30	7'h1E	−66	62	7'h3E	−34	94	7'h5E	−2	126	7'h7E	18
31	7'h1F	−65	63	7'h3F	−33	95	7'h5F	−1	127	7'h7F	18

<Reset Value>
All "7’h00"

<Reset Conditions>
1. At power on resets
2. When putting "1" in the software reset bit RST_A
3. When putting "1" in the software reset bit RST_M

<Access During Power Save State>
Not allowed

7.6.1.7 ADI[0/1/2]_VSEP

MA_REG	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#14 (0x0E)	W	ADI0_VSEP	ADI0_VOL0[6:0]						
#16 (0x10)	W	ADI1_VSEP	ADI1_VOL0[6:0]						
#18 (0x12)	W	ADI2_VSEP	ADI2_VOL0[6:0]						

<Description>

Use this write-only register bit ADI*m*_VSEP for each of ports [0/1/2] to control how input volume level change tracks each other. The *m* in ADI*m*_VSEP maps to the logical port number #0 through #2.

"0": Writing in ADI[0/1/2]_VOL*0* to change volume level makes ADI[0/1/2]_VOL*1* level changed to the same level.
Writing in ADI[0/1/2]_VOL*1* just changes ADI[0/1/2]_VOL*1* level. (Default)

"1": Writing in ADI[0/1/2]_VOL*1* to change volume level makes ADI[0/1/2]_VOL*0* level changed to the same level.
Writing in ADI[0/1/2]_VOL*0* just changes ADI[0/1/2]_VOL*0* level.

<Reset Value>

All "0"

<Reset Conditions>

1. At power on resets
2. When putting "1" in the software reset bit RST_A
3. When putting "1" in the software reset bit RST_M

<Access During Power Save State>

Not allowed

7.6.1.8 ADI[0/1/2]_VOL[0/1]

MA_REG	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#14 (0x0E)	W/R	ADI0_VSEP	ADI0_VOL0[6:0]						
#15 (0x0F)	W/R	"0"	ADI0_VOL1[6:0]						
#16 (0x10)	W/R	ADI1_VSEP	ADI1_VOL0[6:0]						
#17 (0x11)	W/R	"0"	ADI1_VOL1[6:0]						
#18 (0x12)	W/R	ADI2_VSEP	ADI2_VOL0[6:0]						
#19 (0x13)	W/R	"0"	ADI2_VOL1[6:0]						

<Description>

Use these registers to set analog input #[0/1/2] volume levels.
Adjust this register value as input source level changes.
"7'h00": Mute the input
"7'h01" through "7'h72": Attenuate or boost −95 dB through +18 dB in 1 dB step
"7'h72" to "7'h7F": Boost +18 dB
See *7.6.1.6 DIFI[0/1/2/3]_VOL[0/1]* for further information.

<Reset Value>

All "7'h00"

<Reset Conditions>

1. At power on resets
2. When putting "1" in the software reset bit RST_A
3. When putting "1" in the software reset bit RST_M

<Access During Power Save State>

Not allowed

7.6.1.9 DIFO[0/1/2/3]_VSEP

MA_REG	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#20 (0x14)	W	DIFO0_VSEP	DIFO0_VOL0[6:0]						
#22 (0x16)	W	DIFO1_VSEP	DIFO1_VOL0[6:0]						
#24 (0x18)	W	DIFO2_VSEP	DIFO2_VOL0[6:0]						
#26 (0x1A)	W	DIFO3_VSEP	DIFO3_VOL0[6:0]						

<Description>

Use this write-only register bit DIFO*m*_VSEP for each of ports [0/1/2/3] to control how output volume level change tracks each other. The *m* in DIFO*m*_VSEP maps to the logical port number #0 through #3.

"0": Writing in DIFO[0/1/2/3]_VOL*0* to change volume level makes DIFO[0/1/2/3]_VOL*1* level changed to the same level.
Writing in DIFO[0/1/2/3]_VOL*1* just changes DIFO[0/1/2/3]_VOL*1* level. (Default)

"1": Writing in DIFO[0/1/2/3]_VOL*1* to change volume level makes DIFO[0/1/2/3]_VOL*0* level changed to the same level.
Writing in DIFO[0/1/2/3]_VOL*0* just changes DIFO[0/1/2/3]_VOL*0* level.

<Reset Value>

All "0"

<Reset Conditions>

1. At power on resets
2. When putting "1" in the software reset bit RST_A
3. When putting "1" in the software reset bit RST_M

<Access During Power Save State>

Not allowed

7.6.1.10 DIFO[0/1/2/3]_VOL[0/1]

MA_REG	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#20 (0x14)	W/R	DIFO0_VSEP	DIFO0_VOL0[6:0]						
#21 (0x15)	W/R	"0"	DIFO0_VOL1[6:0]						
#22 (0x16)	W/R	DIFO1_VSEP	DIFO1_VOL0[6:0]						
#23 (0x17)	W/R	"0"	DIFO1_VOL1[6:0]						
#24 (0x18)	W/R	DIFO2_VSEP	DIFO2_VOL0[6:0]						
#25 (0x19)	W/R	"0"	DIFO2_VOL1[6:0]						
#26 (0x1A)	W/R	DIFO3_VSEP	DIFO3_VOL0[6:0]						
#27 (0x1B)	W/R	"0"	DIFO3_VOL1[6:0]						

<Description>

Use these registers to set digital audio output #[0/1/2/3] volume levels.

"7'h00": Mute the output

"7'h01" through "7'h72": Attenuate or boost −95 dB through +18 dB in 1 dB step

"7'h72" to "7'h7F": Boost +18 dB

See *7.6.1.6 DIFI[0/1/2/3]_VOL[0/1]* for further information.

<Reset Value>

All "7'h00"

<Reset Conditions>

1. At power on resets
2. When putting "1" in the software reset bit RST_A
3. When putting "1" in the software reset bit RST_M

<Access During Power Save State>

Not allowed

7.6.1.11 DAO[0/1]_VSEP

MA_REG	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#28 (0x1C)	W	DAO0_VSEP	DAO0_VOL0[6:0]						
#30 (0x1E)	W	DAO1_VSEP	DAO1_VOL0[6:0]						

<Description>

Use this write-only register bit DAO*m*_VSEP for each of ports [0/1] to control how output volume level change tracks each other. The *m* in DAO*m*_VSEP maps to the logical port number #0 through #1.

"0": Writing in DAO[0/1]_VOL*0* to change volume level makes DAO[0/1]_VOL*1* level changed to the same level.
Writing in DAO[0/1]_VOL*1* just changes DAO[0/1]_VOL*1* level. (Default)

"1": Writing in DAO[0/1]_VOL*1* to change volume level makes DAO[0/1]_VOL*0* level changed to the same level.
Writing in DAO[0/1]_VOL*0* just changes DAO[0/1]_VOL*0* level.

<Reset Value>

All "0"

<Reset Conditions>

1. At power on resets
2. When putting "1" in the software reset bit RST_A
3. When putting "1" in the software reset bit RST_M

<Access During Power Save State>

Not allowed

7.6.1.12 DAO[0/1]_VOL[0/1]

MA_REG	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#28 (0x1C)	W/R	DAO0_VSEP	DAO0_VOL0[6:0]						
#29 (0x1D)	W/R	"0"	DAO0_VOL1[6:0]						
#30 (0x1E)	W/R	DAO1_VSEP	DAO1_VOL0[6:0]						
#31 (0x1F)	W/R	"0"	DAO1_VOL1[6:0]						

<Description>

Use these registers to set analog output #[0/1] volume levels.

"7'h00": Mute the output

"7'h01" through "7'h72": Attenuate or boost −95 dB through +18 dB in 1 dB step

"7'h72" to "7'h7F": Boost +18 dB

See *7.6.1.6 DIFI[0/1/2/3]_VOL[0/1]* for further information.

<Reset Value>

All "7'h00"

<Reset Conditions>

1. At power on resets
2. When putting "1" in the software reset bit RST_A
3. When putting "1" in the software reset bit RST_M

<Access During Power Save State>

Not allowed

7.6.1.13 LINK_LOCK

MA_REG	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#71 (0x47)	W/R	LINK_LOCK	"0"	"0"	"0"	"0"	"0"	"0"	"0"

<Description>

LINK_LOCK register makes volume change smoothing starts of digital inputs and outputs wait valid SRC outputs. When enabled, sound on the digital paths is muted until DPLL is locked.

"0": Do not wait valid SRC outputs. First volume register change starts smoothing (default)
"1": Wait valid SRC outputs. Smoothing starts when SRC starts working

<Reset Value>

"0"

<Reset Conditions>

1. On power−on resets
2. When putting "1" in the software reset bit RST_A
3. When putting "1" in the software reset bit RST_M

<Access During Power Save State>

Not allowed

7.6.2 SWAP

7.6.2.1 ADI[0/1/2]_SWAP

MA_REG	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#32 (0x20)	W/R	"0"	ADI1_SWAP[2:0]			"0"	ADI0_SWAP[2:0]		
#33 (0x21)	W/R	"0"	"0"	"0"	"0"	"0"	ADI2_SWAP[2:0]		

<Description>
Use this register to swap L and R channels on analog input path#[0/1/2].

Table 7.7. Lch/Rch Swap Settings

Setting Value	Lch	Rch
"0"	L	R
"1"	R	L
"2"	MUTE	MUTE
"3"	L−R	R−L
"4"	L+R	L+R
"5"	(L+R)/2	(L+R)/2
"6"	L	L
"7"	R	R

<Reset Value>
All "3'b000"

<Reset Conditions>
1. At power on resets
2. When putting "1" in the software reset bit RST_A
3. When putting "1" in the software reset bit RST_M

<Access During Power Save State>
Not allowed

7.6.2.2 DAO[0/1]_SWAP

MA_REG	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#34 (0x22)	W/R	"0"	DAO1_SWAP[2:0]			"0"	DAO0_SWAP[2:0]		

<Description>
Use this register to swap L and R channels on analog output path #[0/1].

Table 7.8. Lch/Rch Swap Settings

Setting Value	Lch	Rch
"0"	L	R
"1"	R	L
"2"	MUTE	MUTE
"3"	L−R	R−L
"4"	L+R	L+R
"5"	(L+R)/2	(L+R)/2
"6"	L	L
"7"	R	R

<Reset Value>
All "3'b000"

<Reset Conditions>
1. At power on resets
2. When putting "1" in the software reset bit RST_A
3. When putting "1" in the software reset bit RST_M

<Access During Power Save State>
Not allowed

7.6.3 MIXER

Figure below shows the block diagram for the mixer.
The direction of signal flow is indicated by arrows.
Signals shown in purple and bold indicate control register names.

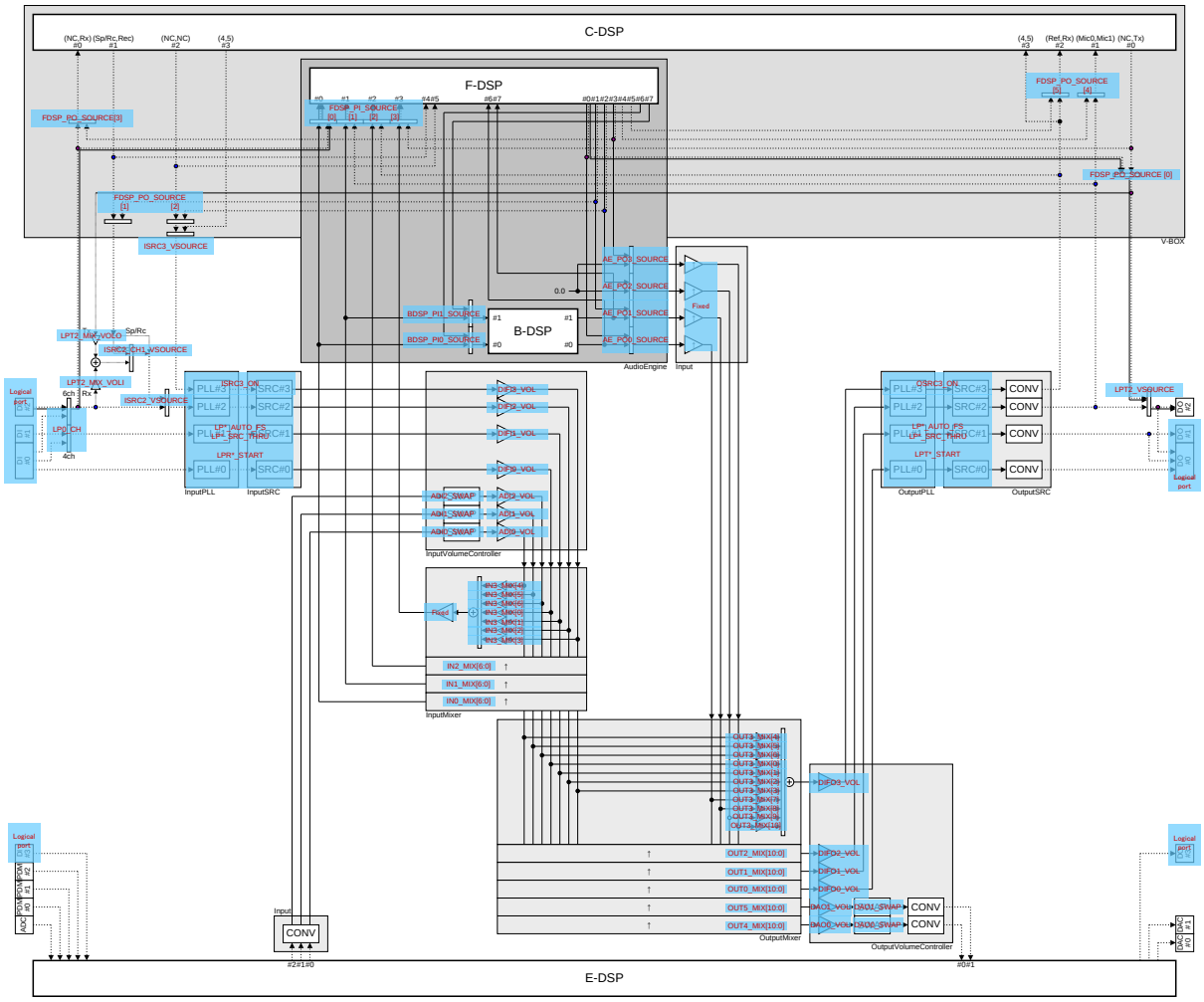


Figure 7-3. MIXER block diagram.

7.6.3.1 IN[0/1/2/3]_MSEP

MA_REG	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#35 (0x23)	W	IN0_MSEP	IN0_MIX0[6:0]						
#37 (0x25)	W	IN1_MSEP	IN1_MIX0[6:0]						
#39 (0x27)	W	IN2_MSEP	IN2_MIX0[6:0]						
#41 (0x29)	W	IN3_MSEP	IN3_MIX0[6:0]						

<Description>

Use this write-only register bit IN*m*_MSEP for each of ports [0/1/2/3] to control how input volume level change tracks each other. The *m* in IN*m*_MSEP maps to the logical port number #0 through #3.

"0": Writing in IN[0/1/2/3]_MIX*0* to change volume level makes IN[0/1/2/3]_MIX*1* level changed to the same level.
Writing in IN[0/1/2/3]_MIX*1* just changes IN[0/1/2/3]_MIX*1* level. (Default)

"1": Writing in IN[0/1/2/3]_MIX*1* to change volume level makes IN[0/1/2/3]_MIX*0* level changed to the same level.
Writing in IN[0/1/2/3]_MIX*0* just changes IN[0/1/2/3]_MIX*0* level.

<Reset Value>

All "0"

<Reset Conditions>

1. At power on resets
2. When putting "1" in the software reset bit RST_A
3. When putting "1" in the software reset bit RST_M

<Access During Power Save State>

Not allowed

7.6.3.2 IN[0/1/2/3]_MIX[0/1]

MA_REG	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#35 (0x23)	W/R	IN0_MSEP	IN0_MIX0[6:0]						
#36 (0x24)	W/R	"0"	IN0_MIX1[6:0]						
#37 (0x25)	W/R	IN1_MSEP	IN1_MIX0[6:0]						
#38 (0x26)	W/R	"0"	IN1_MIX1[6:0]						
#39 (0x27)	W/R	IN2_MSEP	IN2_MIX0[6:0]						
#40 (0x28)	W/R	"0"	IN2_MIX1[6:0]						
#41 (0x29)	W/R	IN3_MSEP	IN3_MIX0[6:0]						
#42 (0x2A)	W/R	"0"	IN3_MIX1[6:0]						

<Description>

Each channel on digital audio path #[0/1/2/3] can be routed to the mixer or not.

"0": Do not route to the mixer (Default)

"1": Route to the mixer

Which path each IN[0/1/2/3]_... controls is shown below, and ..._MIX0 is for CH0 or L channel, and .._MIX1 is for CH1 or R channel.

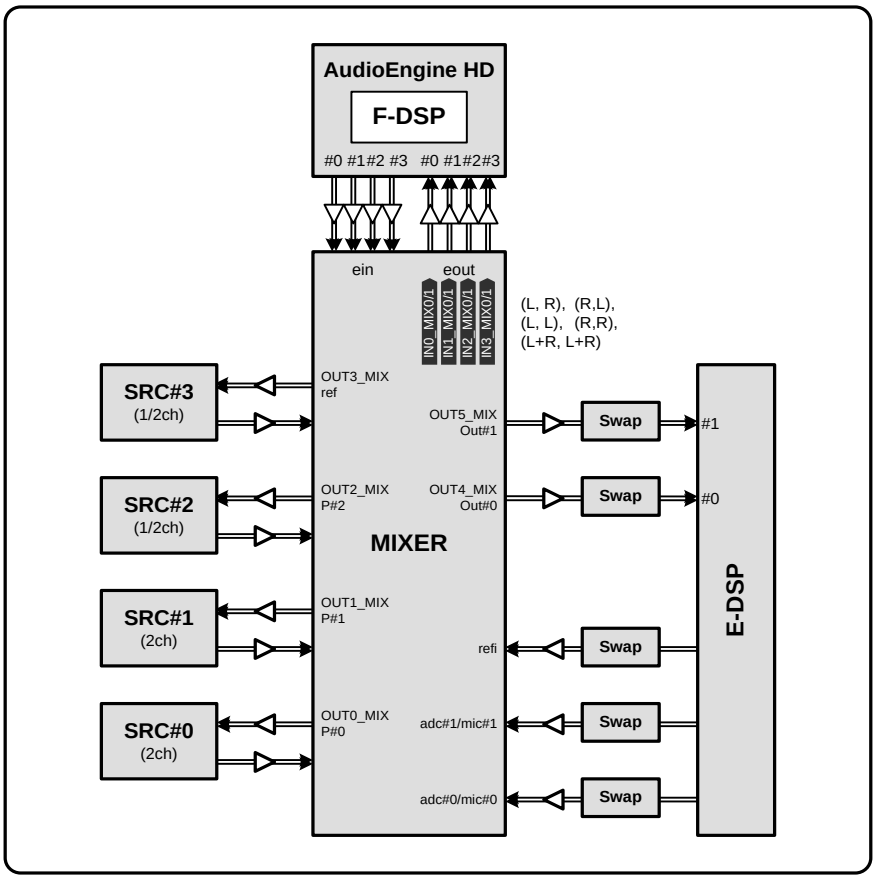


Figure 7-4. MIXER audio paths

NOTICE

Switching between sources without muting output may result in noise.

Table below shows the relationship between register bits and sources.

Table 7.9. The relationship between register bits and sources

BIT	Source
[6]	ADI #2
[5]	ADI #1
[4]	ADI #0
[3]	DIFI #3
[2]	DIFI #2
[1]	DIFI #1
[0]	DIFI #0

<Reset Value>
All "7'h00"

<Reset Conditions>
1. At power on resets
2. When putting "1" in the software reset bit RST_A
3. When putting "1" in the software reset bit RST_M

<Access During Power Save State>
Not allowed

7.6.3.3 OUT[0/.../5]_MSEP

MA_REG	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#43 (0x2B)	W	OUT0_MSEP	"0"	"0"	"0"	"0"	OUT0_MIX0[10:8]		
#47 (0x2F)	W	OUT1_MSEP	"0"	"0"	"0"	"0"	OUT1_MIX0[10:8]		
#51 (0x33)	W	OUT2_MSEP	"0"	"0"	"0"	"0"	OUT2_MIX0[10:8]		
#55 (0x37)	W	OUT3_MSEP	"0"	"0"	"0"	"0"	OUT3_MIX0[10:8]		
#59 (0x3B)	W	OUT4_MSEP	"0"	"0"	"0"	"0"	OUT4_MIX0[10:8]		
#63 (0x3F)	W	OUT5_MSEP	"0"	"0"	"0"	"0"	OUT5_MIX0[10:8]		

<Description>

Use this write-only register bit OUT*m*_MSEP for each of ports [0/.../5] to control how output volume level change tracks each other. The *m* in OUT*m*_MSEP maps to the logical port number #0 through #5.

"0": Writing in OUT[0/.../5]_MIX*0* to change volume level makes OUT[0/.../5]_MIX*1* level changed to the same level.
Writing in OUT[0/.../5]_MIX*1* just changes OUT[0/.../5]_MIX*1* level. (Default)

"1": Writing in OUT[0/.../5]_MIX*1* to change volume level makes OUT[0/.../5]_MIX*0* level changed to the same level.
Writing in OUT[0/.../5]_MIX*0* just changes OUT[0/.../5]_MIX*0* level.

<Reset Value>

All "0"

<Reset Conditions>

1. At power on resets
2. When putting "1" in the software reset bit RST_A
3. When putting "1" in the software reset bit RST_M

<Access During Power Save State>

Not allowed

With "0" being set, value in OUT[0/.../5]_MIX0[10:0] and OUT[0/.../5]_MIX1[10:0] are updated when values are set to lower bytes, OUT[0/.../5]_MIX0[7:0].

With "1" being set, values in OUT[0/.../5]_MIX0[10:0] and OUT[0/.../5]_MIX1[10:0] are updated when values are set to lower bytes, OUT[0/.../5]_MIX1[7:0].

7.6.3.4 OUT[0/.../5]_MIX[0/1]

MA_REG	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#43 (0x2B)	W/R	OUT0_MSEP	"0"	"0"	"0"	"0"	OUT0_MIX0[10:8]		
#44 (0x2C)	W/R	OUT0_MIX0[7:0]							
#45 (0x2D)	W/R	"0"	"0"	"0"	"0"	"0"	OUT0_MIX1[10:8]		
#46 (0x2E)	W/R	OUT0_MIX1[7:0]							
#47 (0x2F)	W/R	OUT1_MSEP	"0"	"0"	"0"	"0"	OUT1_MIX0[10:8]		
#48 (0x30)	W/R	OUT1_MIX0[7:0]							
#49 (0x31)	W/R	"0"	"0"	"0"	"0"	"0"	OUT1_MIX1[10:8]		
#50 (0x32)	W/R	OUT1_MIX1[7:0]							
#51 (0x33)	W/R	OUT2_MSEP	"0"	"0"	"0"	"0"	OUT2_MIX0[10:8]		
#52 (0x34)	W/R	OUT2_MIX0[7:0]							
#53 (0x35)	W/R	"0"	"0"	"0"	"0"	"0"	OUT2_MIX1[10:8]		
#54 (0x36)	W/R	OUT2_MIX1[7:0]							
#55 (0x37)	W/R	OUT3_MSEP	"0"	"0"	"0"	"0"	OUT3_MIX0[10:8]		
#56 (0x38)	W/R	OUT3_MIX0[7:0]							
#57 (0x39)	W/R	"0"	"0"	"0"	"0"	"0"	OUT3_MIX1[10:8]		
#58 (0x3A)	W/R	OUT3_MIX1[7:0]							
#59 (0x3B)	W/R	OUT4_MSEP	"0"	"0"	"0"	"0"	OUT4_MIX0[10:8]		
#60 (0x3C)	W/R	OUT4_MIX0[7:0]							
#61 (0x3D)	W/R	"0"	"0"	"0"	"0"	"0"	OUT4_MIX1[10:8]		
#62 (0x3E)	W/R	OUT4_MIX1[7:0]							
#63 (0x3F)	W/R	OUT5_MSEP	"0"	"0"	"0"	"0"	OUT5_MIX0[10:8]		
#64 (0x40)	W/R	OUT5_MIX0[7:0]							
#65 (0x41)	W/R	"0"	"0"	"0"	"0"	"0"	OUT5_MIX1[10:8]		
#66 (0x42)	W/R	OUT5_MIX1[7:0]							

<Description>

This register specifies digital audio output #[0/1/2/3/4/5] sources mixing.

"0": Mixing not used (default)

"1": Mixing used

For the relationship between OUT[0/.../5]_MIX (0/1) and channels, see figure in *7.6.3.2 IN[0/1/2/3]_MIX[0/1].*

OUT[0/.../5]_MIX0:CH0 (Lch),
OUT[0/.../5]_MIX1:CH1 (Rch)

Noise may be generated when switching on and off of sources not muted.

The update timing varies depending on OUT[0/.../5]_MSEP register setting. See *7.6.3.3 OUT[0/.../5]_MSEP* for details.

In writes, 11 bits must be specified in big-endian byte order.

Table below shows the relationship between register bits and sources.

Table 7.10. The relationship between register bits and sources

BIT	Source
[10]	AEO #3
[9]	AEO #2
[8]	AEO #1
[7]	AEO #0
[6]	ADI #2
[5]	ADI #1
[4]	ADI #0
[3]	DIFI #3
[2]	DIFI #2
[1]	DIFI #1
[0]	DIFI #0

AEO: AudioEngine HD output source

<Reset Value>
All "11'h000"

<Reset Conditions>
1. At power on resets
2. When putting "1" in the software reset bit RST_A
3. When putting "1" in the software reset bit RST_M

<Access During Power Save State>
Not allowed

7.7 E_REG Details

7.7.1 Oversampling Filter(OSF)

7.7.1.1 OSF[0/1]_MN

E_REG	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#2 (0x02)	W/R	LPF1_PST_THR	LPF0_PST_THR	LPF1_PRE_THR	LPF0_PRE_THR	OSF1_MN	OSF0_MN	OSF1_ENB	OSF0_ENB

<Description>

OSF[0/1]_MN register switches if oversampling filters on *DAC#0–1* paths work on stereo samples of mono samples. When working on mono samples, the filter takes input from the left channel, filters it, and outputs in both left and right channels.

"0": Stereo
"1": Mono

<Reset Value>

All "0"

<Reset Conditions>

1. On power−on resets
2. When putting "1" in the software reset bit RST_A
3. When putting "1" in the software reset bit RST_M

<Access During Power Save State>

Not allowed

7.7.1.2 OSF[0/1]_ENB

E_REG	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#2 (0x02)	W/R	LPF1_PST_THR	LPF0_PST_THR	LPF1_PRE_THR	LPF0_PRE_THR	OSF1_MN	OSF0_MN	OSF1_ENB	OSF0_ENB

<Description>

OSF[0/1]_ENB register enables or disables each of the oversampling filter and its associated processing on *DAC#0–1* paths.

"0": Disable oversampling filter processing. Output is fixed to zero
"1": Enable oversampling filter processing

<Reset Value>

All "0"

<Reset Conditions>

1. On power−on resets
2. When putting "1" in the software reset bit RST_A
3. When putting "1" in the software reset bit RST_M

<Access During Power Save State>

Not allowed

7.7.1.3 OSF[0/1]_SEL

E_REG	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#8 (0x08)	W/R	"0"	"0"	"0"	"0"	OSF1_SEL[1:0]		OSF0_SEL[1:0]	

<Description>

This register selects oversampling filter types for the path DAC #0–1.

"0": Brick wall (Sharp Roll-Off) / Linear Phase
"1": Slow Roll-Off /Minimum Phase 1
"2": Brick wall (Sharp Roll-Off) / Minimum Phase
"3": Slow Roll-Off / Minimum Phase 2(default)

<Reset Value>

All "2'b11"

<Reset Conditions>

1. At power on resets
2. When putting "1" in the software reset bit RST_A
3. When putting "1" in the software reset bit RST_M

<Access During Power Save State>

Not allowed

7.7.2 DC Blocking Filters

DC blocking filters block direct current components on DAC#0–1, ADC#0–2 paths.

7.7.2.1 DAC_DCC[0/1]_SEL

E_REG	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#3 (0x03)	W/R	"0"	"0"	"0"	"0"	DAC_DCC1 _SEL[1:0]		DAC_DCC0 _SEL[1:0]	

<Description>
This register selects a cutoff frequency of DC blocking filters. (for the path DAC #0–1)

Table 7.11. DC blocking filter cutoff frequency

Setting Value	DAC_DCC1_SEL	DAC_DCC0_SEL
"0"	350 Hz	75 Hz
"1"	75 Hz	1.8 Hz
"2" (default)	1.8 Hz	1 Hz
"3"	OFF	OFF

<Reset Value>
All "2'b10"

<Reset Conditions>
1. At power on resets
2. When putting "1" in the software reset bit RST_A
3. When putting "1" in the software reset bit RST_M

<Access During Power Save State>
Not allowed

7.7.2.2 ADC_DCC[0/1/2]_SEL

E_REG	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#48 (0x30)	W/R	"0"	"0"	ADC_DCC2 _SEL[1:0]		ADC_DCC1 _SEL[1:0]		ADC_DCC0 _SEL[1:0]	

<Description>

This register selects a cutoff frequency of DC blocking filters. (for the path ADC #0–2)

"0": 75 Hz
"1": 10 Hz (default)
"2": 3 Hz
"3": OFF

<Reset Value>

All "2'b01"

<Reset Conditions>

1. At power on resets
2. When putting "1" in the software reset bit RST_A
3. When putting "1" in the software reset bit RST_M

<Access During Power Save State>

Not allowed

7.7.3 PDM Interface

7.7.3.1 PDM_STWAIT

E_REG	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#71 (0x47)	W/R	"0"	"0"	"0"	"0"	PDM_STWAIT[1:0]		PDM_MODE[1:0]	

<Description>

PDM_STWAIT registers specify a wait time after *PDM[0/1]_START* registers become "1" to ignore input samples. Start sending clocks on the interface makes some digital microphones send invalid samples, so use this register to ignore them.

"0": No wait
"1": 1 ms
"2": 10 ms (default)
"3": 20 ms

<Reset Value>

"2'b10"

<Reset Conditions>

1. On power−on resets
2. When putting "1" in the software reset bit RST_A
3. When putting "1" in the software reset bit RST_M

<Access During Power Save State>

Not allowed

7.7.3.2 PDM_MODE

E_REG	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#71 (0x47)	W/R	"0"	"0"	"0"	"0"	PDM_STWAIT[1:0]		PDM_MODE[1:0]	

<Description>
PDM_MODE register selects digital microphone interface clock output frequency (*PA/DMCK*)

"0": 3.072 MHz (= 64fs$_{_SY}$) (default)
"1": 6.144 MHz (= 128fs$_{_SY}$)
"2": 3.072 MHz (= 64fs$_{_SY}$)
"3": 1.536 MHz (= 32fs$_{_SY}$)

<Reset Value>
"2'b00"

<Reset Conditions>
1. On power−on resets
2. When putting "1" in the software reset bit RST_A
3. When putting "1" in the software reset bit RST_M

<Access During Power Save State>
Not allowed

7.7.3.3 PDM[0/1]_START

E_REG	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#72 (0x48)	W/R	PDM1_ START	PDM1_LOAD_TIM[2:0]			PDM0_ START	PDM0_LOAD_TIM[2:0]		

<Description>

PDM[0/1]_START register starts and stops digital microphone interfaces. Note, starting the interface needs *DSF[0/1/2]_ENB* register (E_REG#41, 43, 45) to be set.

"0": Stop (default)
"1": Start

<Reset Value>

All "0"

<Reset Conditions>

1. On power−on resets
2. When putting "1" in the software reset bit RST_A
3. When putting "1" in the software reset bit RST_M

<Access During Power Save State>

Not allowed

7.7.3.4 PDM[0/1]_LOAD_TIM

E_REG	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#72 (0x48)	W/R	PDM1_START	PDM1_LOAD_TIM[2:0]			PDM0_START	PDM0_LOAD_TIM[2:0]		

<Description>

PDM[0/1]_LOAD_TIM register selects what *DMCK* clock timing is used to sample *DMDIN* signal in on the digital microphone interface.

Table 7.12. DMDIN Signal Fetch Timing

Select	Sample timing
"0"	On *DMCK* rising edge
"1"	On 27 ns before *DMCK* rising edge
"2"	On 27 ns after *DMCK* rising edge
"3"	On 54 ns before *DMCK* rising edge
"4"	On 54 ns after *DMCK* rising edge
"5"	On 81 ns before *DMCK* rising edge
"6"	On 81 ns after *DMCK* rising edge
"7"	On 108 ns before *DMCK* rising edge

The selects "5"–"7" cannot be used when running on 128fs.

The select timings are shown below with a 128fs example.

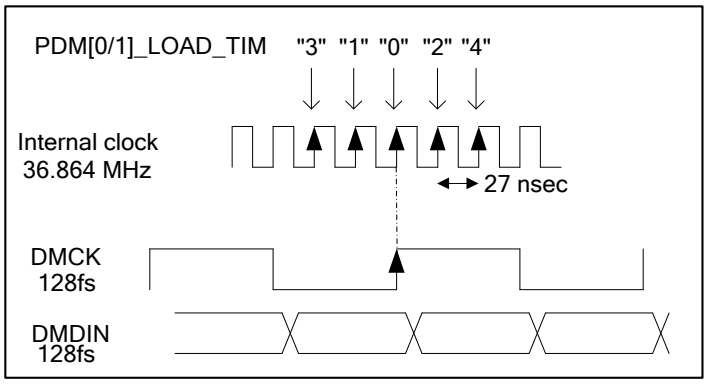


Figure 7-5. Digital microphone interface (128fs).

<Reset Value>

All "3'b000"

<Reset Conditions>

1. On power−on resets
2. When putting "1" in the software reset bit RST_A
3. When putting "1" in the software reset bit RST_M

<Access During Power Save State>

Not allowed

Set "1" to this register when an ADX path is used.

7.7.3.5 PDM0[L/R]_FINE_DLY, PDM1[L/R]_FINE_DLY

E_REG	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#73 (0x49)	W/R	"0"	"0"	PDM0L_FINE_DLY[5:0]					
#74 (0x4A)	W/R	"0"	"0"	PDM0R_FINE_DLY[5:0]					
#75 (0x4B)	W/R	"0"	"0"	PDM1L_FINE_DLY[5:0]					
#76 (0x4C)	W/R	"0"	"0"	PDM1R_FINE_DLY[5:0]					

<Description>

PDM[0/1][L/R]_FINE_DLY registers specify a delay in *sample time* to adjust the phase difference among digital microphone inputs. The downsampling filter gets input samples delayed by the amount specified in these registers. One *sample time* is determined by the frequency set in *PDM_MODE* register.

<Reset Value>

All "6'h00"

<Reset Conditions>

1. On power−on resets
2. When putting "1" in the software reset bit RST_A
3. When putting "1" in the software reset bit RST_M

<Access During Power Save State>

Not allowed

7.8 ANA_REG Details

7.8.1 Hardware ID

7.8.1.1 ANA_ID

ANA_REG	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#0 (0x00)	R	ANA_ID[7:0]							

<Description>
This register shows hardware ID and chip revision. Read only.

<Reset Value>
"8'hA0"

<Reset Conditions>
—

<Access During Power Save State>
Allowed

7.8.2 Soft Reset

7.8.2.1 ANA_RST

ANA_REG	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#1 (0x01)	W/R	"0"	"0"	"0"	"0"	"0"	"0"	"0"	ANA_RST

<Description>
This register bit allows software programs to initialize ANA_REG registers in analog part.
Putting "1" in this bit resets all the ANA_REG registers except this bit.
Put "1" in both of ANA_RST and CD_RST bits to reset all the registers (except those in the host controller interface) in analog part.
"0": Software reset released
"1": Software reset applied (default)

<Reset Value>
"1"

<Reset Conditions>
At power on resets

<Access During Power Save State>
Allowed

7.8.3 Power Management

7.8.3.1 AP_LDOA

ANA_REG	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#2 (0x02)	W/R	"0"	"0"	"0"	AP_ LDOA	AP_ LDO12	"0"	"1"	AP_ VR

<Description>
This register bit enables or disables built-in low dropout regulator LDOA.
When enabling (putting 0 in this bit) the regulator, wait 3 ms before going on.
"0": ON
"1": OFF (default)

<Reset Value>
"1"

<Reset Conditions>
1. At power on resets
2. When putting "1" in the software reset bit ANA_RST

<Access During Power Save State>
Allowed

7.8.3.2 AP_LDO12

ANA_REG	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#2 (0x02)	W/R	"0"	"0"	"0"	AP_ LDOA	AP_ LDO12	"0"	"1"	AP_ VR

<Description>
This register bit enables or disables built-in low dropout regulator LDO12.
When enabling (putting 0 in this bit) the regulator, wait 1 ms before going on.
"0": ON
"1": OFF (default)

<Reset Value>
"1"

<Reset Conditions>
1. At power on resets
2. When putting "1" in the software reset bit ANA_RST

<Access During Power Save State>
Allowed

7.8.3.3 AP_VR

ANA_REG	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#2 (0x02)	W/R	"0"	"0"	"0"	AP_LDOA	AP_LDO12	"0"	"1"	AP_VR

<Description>
This register bit selects ON or OFF for VREF.
"0": ON
"1": OFF (default)

<Reset Value>
"1"

<Reset Conditions>
1. At power on resets
2. When putting "1" in the software reset bit ANA_RST

<Access During Power Save State>
Allowed

7.8.3.4 AP_MC[1/2/3/4]

ANA_REG	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#6 (0x06)	W/R	AP_MC4	AP_MC3	AP_MC2	AP_MC1	"0"	AP_MB3	AP_MB2	AP_MB1

<Description>
This register bit selects ON or OFF for the microphone input blocks (MIC[1/2/3/4]).
AP_MC1 bit corresponds to MIC1, AP_MC2 bit to MIC2, AP_MC3 bit to MIC3, and AP_MC4 bit toMIC4.
"0": ON
"1": OFF (default)

<Reset Value>
All "1"

<Reset Conditions>
1. At power on resets
2. When putting "1" in the software reset bit ANA_RST

<Access During Power Save State>
Allowed

7.8.3.5 AP_MB[1/2/3]

ANA_REG	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#6 (0x06)	W/R	AP_MC4	AP_MC3	AP_MC2	AP_MC1	"0"	AP_MB3	AP_MB2	AP_MB1

<Description>
This register bit selects ON or OFF for microphone bias (MBS[1/2/3]).
AP_MB1 bit corresponds to MBS1, AP_MB2 bit to MBS2, and AP_MB3 bit to MBS3.
"0": ON
"1": OFF (default)

<Reset Value>
All "1"

<Reset Conditions>
1. At power on resets
2. When putting "1" in the software reset bit ANA_RST

<Access During Power Save State>
Allowed

7.8.3.6 AP_AD[L/R/M/X]

ANA_REG	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#7 (0x07)	W/R	"0"	"0"	"0"	"0"	"0"	AP_ ADM	AP_ ADR	AP_ ADL
#55 (0x37)	W/R	AP_ LDOCP	"1"	"0"	"0"	"0"	"0"	"0"	AP_ ADX

<Description>
Use these registers to switch each AD converter block (ADC_[L/R/M/X]) on or off.
AP_ADL switches Lch ADC; AP_ADR, Rch; AP_ADM, Mch (the third channel); and AP_ADX, Xch (the fourth channel).
Wait for 75 ms right after this bit is set to "0" (ON).
"0": ON
"1": OFF (default)

<Reset Value>
All "1"

<Reset Conditions>
1. At power on resets
2. When putting "1" in the software reset bit ANA_RST

<Access During Power Save State>
Allowed

7.8.3.7 AP_LDOCP

ANA_REG	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#55 (0x37)	W/R	AP_ LDOCP	"1"	"0"	"0"	"0"	"0"	"0"	AP_ ADX

<Description>
Use this register to switch the on-chip LDOCP on or off.
"0": ON
"1": OFF (default)

<Reset Value>
"1"

<Reset Conditions>
1. At power on resets
2. When putting "1" in the software reset bit ANA_RST

<Access During Power Save State>
Allowed

7.8.3.8 LO1[L/R]_BUSY, LO2[L/R]_BUSY

ANA_REG	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#12 (0x0C)	R	LO2R_ BUSY	LO2L_ BUSY	LO1R_ BUSY	LO1L_ BUSY	"0"	"0"	"0"	"0"

<Description>
These registers show line out volume interpolation and output offset cancel processing status. Read only.
LO1[L/R]_BUSY bit corresponds to LINEOUT1 Lch/Rch and LO2[L/R]_BUSY bit to LINEOUT2 Lch/Rch.
"0": Processing completed
"1": Processing in progress

<Reset Value>
All "0"

<Reset Conditions>
1. At power on resets
2. When putting "1" in the software reset bit ANA_RST

<Access During Power Save State>
Allowed

7.8.3.9 VREF_RDY

ANA_REG	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#45 (0x2D)	R	"0"	VREF_RDY	"0"	"0"	"0"	"0"	"0"	"0"

<Description>
This register bit indicates VREF voltage has reached its nominal value. Read only.
You can read "1" from the register when the VREF reaches the voltage.
"0": Not ready
"1": Ready.

<Reset Value>
"0"

<Reset Conditions>
1. At power on resets
2. When putting "1" in the software reset bit ANA_RST

<Access During Power Save State>
Allowed

7.8.3.10 LO[1/2]RDY_[L/R]

ANA_REG	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#46 (0x2E)	R	LO2RDY_R	LO2RDY_L	LO1RDY_R	LO1RDY_L	"0"	"0"	"0"	"0"

<Description>

This register bit indicates the offset cancelling on line out pins (LINEOUT[1/2]) has completed. Read only.

LO1RDY_[L/R] bit corresponds to LINEOUT1 Lch/Rch and LO2RDY_[L/R] bit toLINEOUT2 Lch/Rch.

"0": Not ready or the offset cancelling not implemented

"1": Ready

<Reset Value>

All "0"

<Reset Conditions>

1. At power on resets
2. When putting "1" in the software reset bit ANA_RST

<Access During Power Save State>

Allowed

7.8.3.11 LDO[A/18/CP/12]_RDY

ANA_REG	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#57 (0x39)	R	LDOCP_RDY	LDO18_RDY	"0"	LDOA_RDY	LDO12_RDY	MBS3_RDY	MBS2_RDY	MBS1_RDY

<Description>

These read-only registers show if each LDO regulator is ready for use or not.

"0": Not ready

"1": Ready

<Reset Value>

All "0"

<Reset Conditions>

1. At power on resets
2. When putting "1" in the software reset bit ANA_RST

<Access During Power Save State>

Allowed

7.8.4 Mic Bias Controls

7.8.4.1 MBSEL[1/2/3]

ANA_REG	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#13 (0x0D)	W/R	"0"	"0"	MBSEL3[1:0]		MBSEL2[1:0]		MBSEL1[1:0]	

<Description>
Each register selects a microphone bias (MBS[1/2/3]).
MBSEL1 bit corresponds to MBS1, MBSEL2 bit to MBS2, and MBSEL3 bit to MBS3.
"0": 2.0 V (default)
"1": Reserved
"2": 2.7 V
"3": 1.8 V

<Reset Value>
All "0"

<Reset Conditions>
1. At power on resets
2. When putting "1" in the software reset bit ANA_RST

<Access During Power Save State>
Allowed

7.8.4.2 MBS[1/2/3]_DISCH

ANA_REG	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#14 (0x0E)	W/R	"0"	MBS3_ DISCH	MBS2_ DISCH	MBS1_ DISCH	"0"	"0"	"0"	"0"

<Description>
Putting "1" in this bit pulls down the microphone bias output (MBS[1/2/3]) to the ground when the microphone is not used.
MBS1_DISCH bit corresponds to MBS1, MBS2_DISCH bit to MBS2, and MBS3_DISCH bit to MBS3.
"0": High impedance state (default)
"1": Microphone bias output pulled down

<Reset Value>
All "0"

<Reset Conditions>
1. At power on resets
2. When putting "1" in the software reset bit ANA_RST

<Access During Power Save State>
Allowed

7.8.5 Pin Function Controls

7.8.5.1 DIF_LO[1/2]

ANA_REG	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#24 (0x18)	W/R	"0"	"0"	DIF_LO2	DIF_LO1	"0"	"0"	"0"	"0"

<Description>
These register bits configure line out pin pairs (LINEOUT[1L/1R/2L/2R]) to be used for stereo signal outputs or for a differential signal output.
DIF_LO1 bit configures LINEOUT1[L/R] pair and DIF_LO2 bit, LINEOUT2[L/R] pair.

"0": Stereo signal outputs (default)
"1": A differential signal output

<Reset Value>
All "0"

<Reset Conditions>
1. At power on resets
2. When putting "1" in the software reset bit ANA_RST

<Access During Power Save State>
Allowed

7.8.5.2 MC[1/2/3/4]SNG

ANA_REG	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#44 (0x2C)	W/R	MC4SNG	MC3SNG	MC2SNG	MC1SNG	"0"	"0"	"0"	"0"

<Description>
Use these register to switch single-ended or differential signaling for microphone input (MIC[1/2/3/4]).
Use MC1SNG for MIC1, MC2SNG for MIC2, and so on.

"0": Differential signaling (default)
"1": Single-ended signaling

<Reset Value>
All "0"

<Reset Conditions>
1. At power on resets
2. When putting "1" in the software reset bit ANA_RST

<Access During Power Save State>
Allowed

7.8.6 VOLUME

7.8.6.1 MC[1/2/3/4]VOL

ANA_REG	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#27 (0x1B)	W/R	"0"	"0"	MC1VOL[5:0]					
#28 (0x1C)	W/R	"0"	"0"	MC2VOL[5:0]					
#29 (0x1D)	W/R	"0"	"0"	MC3VOL[5:0]					
#30 (0x1E)	W/R	"0"	"0"	MC4VOL[5:0]					

<Description>

Use these registers to set microphone input path gains.

MC1VOL: MIC1
MC2VOL: MIC2
MC3VOL: MIC3
MC4VOL: MIC4

AP_MC[1/2/3/4] must be "1" when changing MC[1/2/3/4]VOL.

The value in these register maps to the gain (Mute, −30 dB to +30 dB) as follows.

Table 7.13. Microphone Input Path Gain Setting

Setting value	VOLUME [dB]	Setting value	VOLUME [dB]	Setting value	VOLUME [dB]	Setting value	VOLUME [dB]
0	Mute	16	−17.0	32	−1.0	48	15.0
1	Mute	17	−16.0	33	0.0	49	16.0
2	Mute	18	−15.0	34	1.0	50	17.0
3	−30.0	19	−14.0	35	2.0	51	18.0
4	−29.0	20	−13.0	36	3.0	52	19.0
5	−28.0	21	−12.0	37	4.0	53	20.0
6	−27.0	22	−11.0	38	5.0	54	21.0
7	−26.0	23	−10.0	39	6.0	55	21.5
8	−25.0	24	−9.0	40	7.0	56	22.0
9	−24.0	25	−8.0	41	8.0	57	22.5
10	−23.0	26	−7.0	42	9.0	58	23.0
11	−22.0	27	−6.0	43	10.0	59	23.5
12	−21.0	28	−5.0	44	11.0	60	24.0
13	−20.0	29	−4.0	45	12.0	61	26.0
14	−19.0	30	−3.0	46	13.0	62	28.0
15	−18.0	31	−2.0	47	14.0	63	30.0

<Reset Value>

All "6'h00"

<Reset Conditions>

1. At power on resets
2. When putting "1" in the software reset bit ANA_RST

<Access During Power Save State>

Allowed

7.8.6.2 ALAT_LO[1/2]

ANA_REG	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#36 (0x24)	W/R	ALAT_LO1	LO1VOL_L[6:0]						
#38 (0x26)	W/R	ALAT_LO2	LO2VOL_L[6:0]						

<Description>

With the bit "1", LO[1/2]VOL_L and LO[1/2]VOL_R setting values become available at the same time when LO[1/2]VOL_R is written. Write values to LO[1/2]VOL_L then LO[1/2]VOL_R.
If writes to LO[1/2]VOL_L and ALAT_ LO[1/2] (= "1") occur at the same time, values written to LO[1/2]VOL_L will be available for processing after LO[1/2]VOL_R is written.
With the bit "0", the setting values become available right after each value is written.

<Reset Value>

All "1"

<Reset Conditions>

1. At power on resets
2. When putting "1" in the software reset bit ANA_RST

<Access During Power Save State>

Allowed

7.8.6.3 LO1VOL_[L/R]

ANA_REG	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#36 (0x24)	W/R	ALAT_LO1	LO1VOL_L[6:0]						
#37 (0x25)	W/R	"0"	LO1VOL_R[6:0]						

<Description>
The registers are used for setting volume level for Line Output 1 (LINEOUT1).
LO1VOL_L is provided for Lch, LO1VOL_R Rch.
Table below shows the relationship between setting values and volume level (Mute, −36 dB to 0 dB).

Table 7.14. LINEOUT1 Gain Setting

Setting value	VOLUME [dB]	Setting value	VOLUME [dB]	Setting value	VOLUME [dB]	Setting value	VOLUME [dB]
0	Power Save	32	Mute	64	−19.00	96	−3.75
1	Mute	33		65	−18.00	97	−3.50
2		34		66	−17.00	98	−3.25
3		35		67	−16.00	99	−3.00
4		36		68	−15.50	100	−2.75
5		37	Reserved	69	−15.00	101	−2.50
6		38		70	−14.50	102	−2.25
7		39		71	−14.00	103	−2.00
8		40		72	−13.50	104	−1.75
9		41		73	−13.00	105	−1.50
10		42		74	−12.50	106	−1.25
11		43		75	−12.00	107	−1.00
12		44		76	−11.50	108	−0.75
13		45		77	−11.00	109	−0.50
14		46		78	−10.50	110	−0.25
15		47	−36.00	79	−10.00	111	0.00
16		48	−35.00	80	−9.50	112	Reserved
17		49	−34.00	81	−9.00	113	
18		50	−33.00	82	−8.50	114	
19		51	−32.00	83	−8.00	115	
20		52	−31.00	84	−7.50	116	
21		53	−30.00	85	−7.00	117	
22		54	−29.00	86	−6.50	118	
23		55	−28.00	87	−6.00	119	
24		56	−27.00	88	−5.75	120	
25		57	−26.00	89	−5.50	121	
26		58	−25.00	90	−5.25	122	
27		59	−24.00	91	−5.00	123	
28		60	−23.00	92	−4.75	124	
29		61	−22.00	93	−4.50	125	
30		62	−21.00	94	−4.25	126	
31		63	−20.00	95	−4.00	127	

<Reset Value>
All "7'h00"

<Reset Conditions>
1. At power on resets
2. When putting "1" in the software reset bit ANA_RST

<Access During Power Save State>
Allowed

7.8.6.4 LO2VOL_[L/R]

ANA_REG	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#38 (0x26)	W/R	ALAT_LO2	LO2VOL_L[6:0]						
#39 (0x27)	W/R	"0"	LO2VOL_R[6:0]						

<Description>

The registers are used for setting volume level for Line Output 2 (LINEOUT2).
LO2VOL_L is provided for Lch, LO2VOL_R Rch.
Table below shows the relationship between setting values and volume level (Mute, −36 dB to 0 dB).
See *7.8.6.3 LO1VOL_[L/R]*.

<Reset Value>

All "7'h00"

<Reset Conditions>

1. At power on resets
2. When putting "1" in the software reset bit ANA_RST

<Access During Power Save State>

Allowed

7.8.6.5 SVOL_LO[1/2]

ANA_REG	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#41 (0x29)	W/R	"0"	"0"	"0"	SVOL _LO2	SVOL _LO1	"0"	"0"	"0"

<Description>

SVOL_LO[0/1] registers enable or disable hardware volume change smoothing for volume changes with *LO[1/2]VOL_[L/R]*. *SVOL_LO1* register controls *LINEOUT1* output smoothing while *SVOL_LO2* register controls *LINEOUT2* output smoothing.

"0": Disable volume change smoothing
"1": Enable volume change smoothing (default)

<Reset Value>

All "1"

<Reset Conditions>

1. On power−on resets
2. When putting "1" in the software reset bit ANA_RST

<Access During Power Save State>

Allowed

7.8.7 ANALOG MIXER

7.8.7.1 AD[L/R/M/X]_M[1/2/3/4]MIX

ANA_REG	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#48 (0x30)	W/R	ADL_ M4MIX	ADL_ M3MIX	ADL_ M2MIX	ADL_ M1MIX	"0"	"0"	"0"	"0"
#49 (0x31)	W/R	ADR_ M4MIX	ADR_ M3MIX	ADR_ M2MIX	ADR_ M1MIX	"0"	"0"	"0"	"0"
#50 (0x32)	W/R	ADM_ M4MIX	ADM_ M3MIX	ADM_ M2MIX	ADM_ M1MIX	"0"	"0"	"0"	"0"
#56 (0x32)	W/R	ADX_ M4MIX	ADX_ M3MIX	ADX_ M2MIX	ADX_ M1MIX	"0"	"0"	"0"	"0"

<Description>

This register selects which microphone inputs should be fed to mixers for further processing in AD converter (ADC_[L/R/M/X]).

ADL_M1MIX, for example, is used for MIC1 input mixing for ADC_L.

"0": Mixing not used (default)

"1": Mixing used

<Reset Value>

All "0"

<Reset Conditions>

1. At power on resets
2. When putting "1" in the software reset bit ANA_RST

<Access During Power Save State>

Allowed

7.8.8 CHARGE PUMP

7.8.8.1 LDOCP_LIM_ON

ANA_REG	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#58 (0x3A)	W/R	"0"	"0"	"0"	LDOCP_LIM_ON	"0"	"0"	"0"	"0"

<Description>
Use this register to enable or disable LDOCP output current limiter.

"0": Limiter OFF (default)
"1": Limiter ON

<Reset Value>
"0"

<Reset Conditions>
1. At power on resets
2. When putting "1" in the software reset bit ANA_RST

<Access During Power Save State>
Allowed

7.9 CD_REG Details

7.9.1 Soft Reset

7.9.1.1 CD_RST

CD_REG	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#1 (0x01)	W/R	"0"	"0"	"0"	"0"	"0"	"0"	"0"	CD_RST

<Description>
This register bit allows software programs to initialize CD_REG registers in the analog part.
Putting "1" in this bit initialize all the CD_REG registers but this bit.
Putting "1" in both bits of CD_RST and ANA_RST initializes all the analog part registers (accept those in the host controller interface).
"0": Idle state
"1": Initialize CD_REG registers (default)

<Reset Value>
"1"

<Reset Conditions>
At power on resets

<Access During Power Save State>
Allowed

7.9.2 Power Management

See the table below to configure registers for each signal path and application to enable clocks when starting analog blocks. Setting to "0" enables clock signals. Cells with "0" indicate registers to be set.

Table 7.15. Register Settings for each Signal Path / Application

Register / Signal Path	DP_ ADCX	DP_ ADCLK	DP_ ADOUT	DP_ ADC	DP_ DAC0	DP_ DAC1	DP_ PDMCK	DP_ PDMADC	DP_ PDMDAC
	CD_REG#40			CD_REG#2					
DAC0 (LO1)	*	*	*	*	0	0	0	*	0
DAC1 (LO2)	*	*	*	*	*	0	0	*	0
ADC [L/R/M]	*	*	*	0	*	*	0	0	*
ADC [X]	0	0	0	*	*	*	*	*	*
Offset Cancel	*	*	*	*	0	0	0	0	0

7.9.2.1 DP_ADC

CD_REG	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#2 (0x02)	W/R	"0"	DP_ ADC	DP_ DAC1	DP_ DAC0	"0"	DP_ PDMCK	DP_ PDMADC	DP_ PDMDAC

<Description>
This register bit controls clock signals in ADC block.
This bit must be "0" when using line level inputs, and microphone inputs, and also when using speaker or during output offset cancelling.
"0": Clock running
"1": Clock stopped (default)

<Reset Value>
"1"

<Reset Conditions>
1. At power on resets
2. When putting "1" in the software reset bit CD_RST

<Access During Power Save State>
Allowed

7.9.2.2 DP_DAC[0/1]

CD_REG	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#2 (0x02)	W/R	"0"	DP_ ADC	DP_ DAC1	DP_ DAC0	"0"	DP_ PDMCK	DP_ PDMADC	DP_ PDMDAC

<Description>

This register bit controls clock signals in DAC block (DAC[0/1]).
Put "0" in both DP_DAC0 and DP_DAC1 when using DAC0 path (Headphone / Receiver / Line Out 1).

"0": Clock running
"1": Clock stopped (default)

How DAC0 and DAC1 paths (Speaker/Line Out 2) are used determines which values to use as follows.

Table 7.16. DAC clock setting

		DAC1 Path	
		Used	Not Used
DAC0 Path	Used	DP_DAC0 = "0" DP_DAC1 = "0"	DP_DAC0 = "0" DP_DAC1 = "0"
	Not Used	DP_DAC0 = "1" DP_DAC1 = "0"	DP_DAC0 = "1" DP_DAC1 = "1"

<Reset Value>

All "1"

<Reset Conditions>

1. At power on resets
2. When putting "1" in the software reset bit CD_RST

<Access During Power Save State>

Allowed

7.9.2.3 DP_PDMCK

CD_REG	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#2 (0x02)	W/R	"0"	DP_ ADC	DP_ DAC1	DP_ DAC0	"0"	DP_ PDMCK	DP_ PDMADC	DP_ PDMDAC

<Description>

This bit controls the gating of PDM clock signal coming from digital part to analog part.

"0": Not gated (clock comes from digital part)
"1": Gated (clock not comes from digital part) (default)

<Reset Value>

"1"

<Reset Conditions>

1. At power on resets
2. When putting "1" in the software reset bit CD_RST

<Access During Power Save State>

Allowed

7.9.2.4 DP_PDMADC

CD_REG	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#2 (0x02)	W/R	"0"	DP_ ADC	DP_ DAC1	DP_ DAC0	"0"	DP_ PDMCK	DP_ PDMADC	DP_ PDMDAC

<Description>
This bit controls the gating of PDM data signal going to digital part from analog part.
"0": Not gated (data goes to digital part)
"1": Gated (data not goes to digital part) (default)

<Reset Value>
"1"

<Reset Conditions>
1. At power on resets
2. When putting "1" in the software reset bit CD_RST

<Access During Power Save State>
Allowed

7.9.2.5 DP_PDMDAC

CD_REG	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#2 (0x02)	W/R	"0"	DP_ ADC	DP_ DAC1	DP_ DAC0	"0"	DP_ PDMCK	DP_ PDMADC	DP_ PDMDAC

<Description>
This bit controls the gating of PDM data signal coming from digital part to analog part.
"0": Not gated (data comes from digital part)
"1": Gated (data not comes from digital part) (default)

<Reset Value>
"1"

<Reset Conditions>
1. At power on resets
2. When putting "1" in the software reset bit CD_RST

<Access During Power Save State>
Allowed

7.9.2.6 DP_ADCX

CD_REG	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#40 (0x28)	W/R	"0"	DP_ ADCX	"0"	"0"	"0"	DP_ ADCLK	DP_ ADOUT	"0"

<Description>
Use this register to control ADC_X block clock gating.

"0": Enable the clock to the block
"1": Disable the clock to the block (default)

<Reset Value>
"1"

<Reset Conditions>
1. At power on resets
2. When putting "1" in the software reset bit CD_RST

<Access During Power Save State>
Allowed

7.9.2.7 DP_ADCLK

CD_REG	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#40 (0x28)	W/R	"0"	DP_ ADCX	"0"	"0"	"0"	DP_ ADCLK	DP_ ADOUT	"0"

<Description>
Use this register to control ADCLK block clock gating.

"0": Enable the clock to the block
"1": Diablo the clock to the block (default)

<Reset Value>
"1"

<Reset Conditions>
1. At power on resets
2. When putting "1" in the software reset bit CD_RST

<Access During Power Save State>
Allowed

7.9.2.8 DP_ADOUT

CD_REG	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#40 (0x28)	W/R	"0"	DP_ADCX	"0"	"0"	"0"	DP_ADCLK	DP_ADOUT	"0"

<Description>
Use this register to mask ADOUT pin output.

"0": Enable the output
"1": Mask the output (output fixed) (default)

<Reset Value>
"1"

<Reset Conditions>
1. At power on resets
2. When putting "1" in the software reset bit CD_RST

<Access During Power Save State>
Allowed

7.9.2.9 DP_CLKI

CD_REG	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#41 (0x29)	W/R	"0"	"0"	"0"	"0"	"0"	"0"	"0"	DP_CLKI

<Description>
Use this register to gate the clock fed to the embedded microcontroller from CLKI pin. The gating is valid when the device is in slave mode. You can read and write this register in the master mode, though it does not control the gating.

"0": Enable CLKI clock to the embedded microcontroller (default)
"1": Disable CLKI clock to the embedded microcontroller

<Reset Value>
"0"

<Reset Conditions>
1. At power on resets
2. When putting "1" in the software reset bit CD_RST

<Access During Power Save State>
Allowed

7.9.3 GPIO(GPIO[0/1/2/3]) Pin Controls

7.9.3.1 EIRQGPIO

CD_REG	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#43 (0x2B)	W/R	"0"	"0"	"0"	"0"	EIRQGPIO	"0"	"0"	"0"

<Description>
Use this register to mask those interrupt requests made with GPIO[0/1/2/3] input.
Other requests to the embedded microcontroller (on *Interrupt 1*) will not be masked.

"0": Mask GPIO interrupt requests
"1": Allow GPIO interrupt requests

When this register "1", the signal on those GPIO pins enabled with GPIO[0/1/2/3]_INTE flags interrupts the microcontroller.

<Reset Value>
"0"

<Reset Conditions>
1. At power on resets
2. When putting "1" in the software reset bit CD_RST

<Access During Power Save State>
Allowed

7.9.3.2 GP[0/1/2/3]_INTE

CD_REG	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#44 (0x2C)	W/R	GP0_INTE	"0"	GP0_DDR	GP0_DATA	"0"	"0"	GP0_MSK	GP0_INV
#45 (0x2D)	W/R	GP1_INTE	"0"	GP1_DDR	GP1_DATA	"0"	"0"	GP1_MSK	GP1_INV
#46 (0x2E)	W/R	GP2_INTE	"0"	GP2_DDR	GP2_DATA	"0"	"0"	GP2_MSK	GP2_INV
#47 (0x2F)	W/R	GP3_INTE	"0"	GP3_DDR	GP3_DATA	"0"	"0"	GP3_MSK	GP3_INV

<Description>
Use these register to allow interrupts with GPIO[0/1/2/3] inputs

"0": Do not use the GPIO input for interrupts (default)
"1": Use the GPIO input for interrupts

<Reset Value>
All "0"

<Reset Conditions>
1. At power on resets
2. When putting "1" in the software reset bit CD_RST

<Access During Power Save State>
Allowed

7.9.3.3 GP[0/1/2/3]_DDR

CD_REG	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#44 (0x2C)	W/R	GP0_INTE	"0"	GP0_DDR	GP0_DATA	"0"	"0"	GP0_MSK	GP0_INV
#45 (0x2D)	W/R	GP1_INTE	"0"	GP1_DDR	GP1_DATA	"0"	"0"	GP1_MSK	GP1_INV
#46 (0x2E)	W/R	GP2_INTE	"0"	GP2_DDR	GP2_DATA	"0"	"0"	GP2_MSK	GP2_INV
#47 (0x2F)	W/R	GP3_INTE	"0"	GP3_DDR	GP3_DATA	"0"	"0"	GP3_MSK	GP3_INV

<Description>
Use these registers to configure the port GPIO[0/1/2/3] to be used as an input or output.

"0": Input port (default)
"1": Output port

<Reset Value>
All "0"

<Reset Conditions>
1. At power on resets
2. When putting "1" in the software reset bit CD_RST

<Access During Power Save State>
Allowed

7.9.3.4 GP[0/1/2/3]_DATA

CD_REG	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#44 (0x2C)	W/R	GP0_INTE	"0"	GP0_DDR	GP0_DATA	"0"	"0"	GP0_MSK	GP0_INV
#45 (0x2D)	W/R	GP1_INTE	"0"	GP1_DDR	GP1_DATA	"0"	"0"	GP1_MSK	GP1_INV
#46 (0x2E)	W/R	GP2_INTE	"0"	GP2_DDR	GP2_DATA	"0"	"0"	GP2_MSK	GP2_INV
#47 (0x2F)	W/R	GP3_INTE	"0"	GP3_DDR	GP3_DATA	"0"	"0"	GP3_MSK	GP3_INV

<Description>

・For the port configured as an input (GP[0/1/2/3]_DDR = "0")
This register shows GPIO[0/1/2/3] logic level. The value may be masked or inverted as follows.
GP[0/1/2/3]_MSK (CD_REG #44–47) (to mask)
GP[0/1/2/3]_INV (CD_REG #44–47) (to invert)

・For the port configured as an output (GP[0/1/2/3]_DDR = "1")
GPIO[0/1/2/3] pin is driven to the logic level value in these registers.

<Reset Value>

All "0"

<Reset Conditions>

1. At power on resets
2. When putting "1" in the software reset bit CD_RST

<Access During Power Save State>

Allowed

7.9.3.5 GP[0/1/2/3]_MSK

CD_REG	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#44 (0x2C)	W/R	GP0_INTE	"0"	GP0_DDR	GP0_DATA	"0"	"0"	GP0_MSK	GP0_INV
#45 (0x2D)	W/R	GP1_INTE	"0"	GP1_DDR	GP1_DATA	"0"	"0"	GP1_MSK	GP1_INV
#46 (0x2E)	W/R	GP2_INTE	"0"	GP2_DDR	GP2_DATA	"0"	"0"	GP2_MSK	GP2_INV
#47 (0x2F)	W/R	GP3_INTE	"0"	GP3_DDR	GP3_DATA	"0"	"0"	GP3_MSK	GP3_INV

<Description>

For GPIO[0/1/2/3] configured as an input (GP[0/1/2/3]_DDR = "0"), use these registers to mask the input. Writing GP[0/1/2/3]_MSK "1" masks the GPIO[0/1/2/3] input, makes it always read as "0". These registers are not used when configured as an output (GP[0/1/2/3]_DDR = "1").

"0": Do not mask GPIO[0/1/2/3] input
"1": Mask GPIO[0/1/2/3] input (default)

<Reset Value>

All "1"

<Reset Conditions>

1. At power on resets
2. When putting "1" in the software reset bit CD_RST

<Access During Power Save State>

Allowed

7.9.3.6 GP[0/1/2/3]_INV

CD_REG	W/R	D7	D6	D5	D4	D3	D2	D1	D0
#44 (0x2C)	W/R	GP0_INTE	"0"	GP0_DDR	GP0_DATA	"0"	"0"	GP0_MSK	GP0_INV
#45 (0x2D)	W/R	GP1_INTE	"0"	GP1_DDR	GP1_DATA	"0"	"0"	GP1_MSK	GP1_INV
#46 (0x2E)	W/R	GP2_INTE	"0"	GP2_DDR	GP2_DATA	"0"	"0"	GP2_MSK	GP2_INV
#47 (0x2F)	W/R	GP3_INTE	"0"	GP3_DDR	GP3_DATA	"0"	"0"	GP3_MSK	GP3_INV

<Description>

For the port configured as an input (GP[0/1/2/3]_DDR = "0"), use these registers to invert the logic level found on the GPIO[0/1/2/3] pin.

For the port configured as an output (GP[0/1/2/3]_DDR= "1"), these registers are not used.

"0": Do not invert the port logic level (default)
"1": Invert the port logic level

<Reset Value>

All "0"

<Reset Conditions>

1. At power on resets
2. When putting "1" in the software reset bit CD_RST

<Access During Power Save State>

Allowed

8 Electrical Characteristics

8.1 Absolute Maximum Ratings

$V_{DGND} = V_{AGND} = V_{CPGND} = 0$ V

Parameter		Symbol	Min.	Max.	Unit
Supply Voltage	VDD33	V_{VDD33}	−0.3	4.60	V
	IOVDD1	V_{IOVDD1}			
	IOVDD2	V_{IOVDD2}			
Input Voltage (See Note 1.)	Digital Pins (See Note 3.)	V_{IND1}	V_{DGND} − 0.3	V_{IOVDD1} + 0.3	V
	Digital Pins (See Note 4.)	V_{IND2}		V_{IOVDD2} + 0.3	
	SCL, SDA	V_{INDT}		4.20	
	Analog pins	V_{INA}	V_{AGND} − 0.3	V_{AVDD} + 0.3	
Power dissipation (See Note 2.)		P_D	–	5.1	W
Junction temperature		T_j	–	125	°C
Storage temperature		T_{STG}	−50	125	°C

Note 1: No ratings must be exceeded even when supply voltages are outside the recommended operating voltage range. For example, 0.3 V input violates the rating when supply pins is at 0 V.

Note 2: Ta = 25 °C, using glass epoxy PCB (76.2 mm × 114.3 mm × 1.6 mm)
When operating temperature is above 25 °C, delete the value 51mW for every 1 °C increase.
Use this value only as a guide for your design as these values are for our reference PCB construction and design.

Note 3: MPUE_N, MPURST_N/SPIMODE, SCK, MOSI, SS_N, MISO, ADCLK, ADOUT, BCLK1, LRCK1, SDIN1, SDOUT1, DMCK, DMDIN*, GPIO*, and IRQ_N, TEST*

Note 4: BCLK2, LRCK2, SDIN2, SOUT2

8.2 Recommended Operating Conditions

$V_{DGND} = V_{AGND} = V_{CPGND} = 0$ V

Parameter		Symbol	Min.	Typ.	Max.	Unit
Supply voltage	VDD33	V_{VDD33}	2.80	3.30	3.60	V
	IOVDD1	V_{IOVDD1}				
	IOVDD2 (See Note 1.)	V_{IOVDD2}	2.80	3.30	3.60	
			1.65	1.80	1.95	
Operating ambient temperature (See Note 2.)		T_a	−40	25	85	°C

Note 1: IOVDD2 supports two power supply options.

Note 2: Open air temperature away from the device where the radiation from the device is negligible.

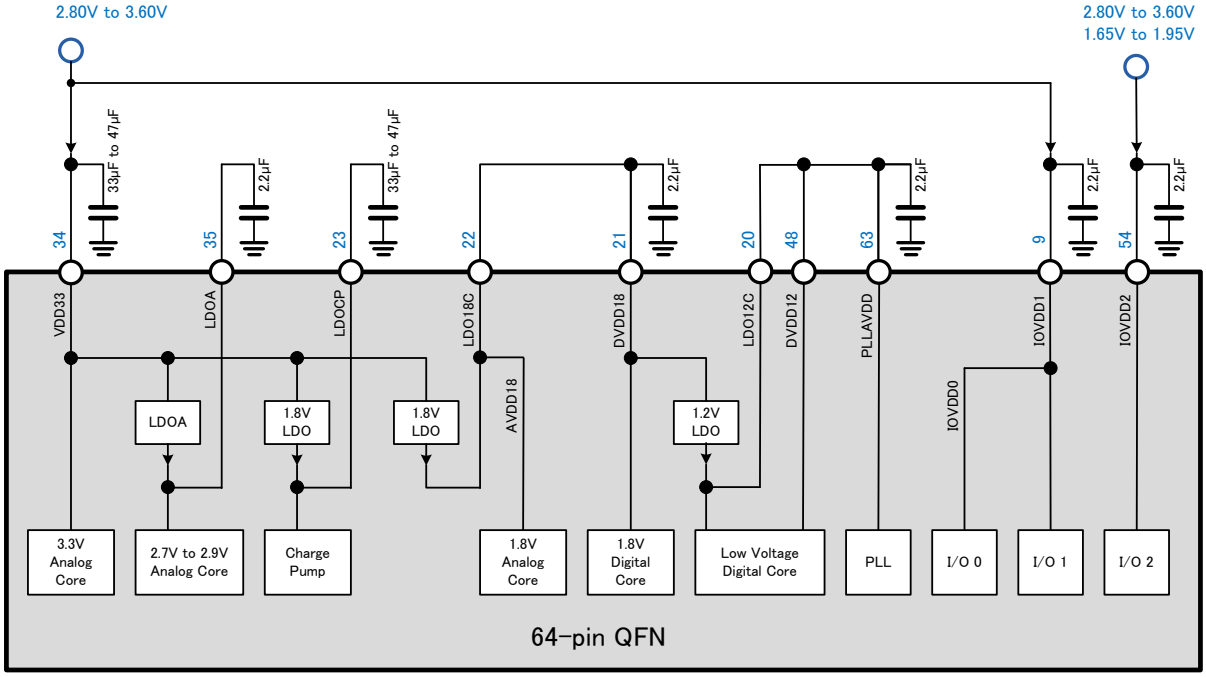


Figure 8-1. Power supply configuration.

8.3 Operating Current

T_a = 25°C, V_{VDD33} = V_{IOVDD1} = V_{IOVDD2} = 3.3V

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
In normal mode	I_{OP}	(See Note 1.)	–	4	–	mA
		(See Note 2.)	–	8.5	–	mA
When stopped	I_{PS}	(See Note 3.)	–	84	–	μA

Note 1: SPI slave mode, Digital Audio Input (no sound) → DAC→ LINEOUT1[L/R] (no load), DSP off
Audio I/F: I^2S slave mode, Sampling Frequency = 48 kHz, Bit Clock Frequency = 64fs

Note 2: SPI master mode, MIC1 (no sound) → ADC → DAC → LINEOUT1L (no load), DSP off
MBS1 = 2.0 V

Note 3: ANA_RST = CD_RST = "1", All inputs including CLKI are being stopped

8.4 DC Characteristics

Capacitive load = 50 pF within the recommended operating conditions

Parameter		Symbol	Description	Min.	Typ.	Max.	Unit
Digital input voltage	"H"	V_{IH}	SDIN2, LRCK2, BCLK2	0.70 × V_{IOVDD2}	–	–	V
	"L"	V_{IL}		–		0.30 × V_{IOVDD2}	
	"H"	V_{IH}	Other digital inputs	0.70 × V_{IOVDD1}	–	–	
	"L"	V_{IL}		–		0.30 × V_{IOVDD1}	
Digital output voltage	"H"	V_{OH}	SDOUT2, LRCK2, BCLK2	0.80 × V_{IOVDD2}	–	–	V
	"L"	V_{OL}		–		0.20 × V_{IOVDD2}	
	"H"	V_{OH}	Other digital outputs (See Note 1.)	0.80 × V_{IOVDD1}	–	–	
	"L"	V_{OL}		–		0.20 × V_{IOVDD1}	
	"L"	V_{OL}	IRQ_N (I_{OL}= +2 mA)	–	–	0.20 × V_{IOVDD1}	
	"L"	V_{OL}	SDA (I_{OL}= +3 mA)	–	–	0.4	
Schmitt width		V_{SH1}	CLKI, SCK, SS_N, MOSI, MISO, ADCLK, GPIO[0,1,2,3]	–	0.05 × V_{IOVDD1}	–	V
		V_{SH2}	SCL, SDA		0.05 × V_{IOVDD1}		
Input leakage current		I_L	CLKI, SCK, TEST0	–	–	±2.0	μA
			Other inputs			±1.0	
Input capacitance		C_I	CLKI, SCK, TEST0	–	–	20	pF
			Other inputs			10	

Note 1: I_{OH}= -1mA, I_{OL}= +1mA

8.5 AC Characteristics

8.5.1 Power-on rule, Input signal slope rule

Within the recommended operating conditions

Parameter		Symbol	Min.	Typ.	Max.	Unit
Power	Power supply rise time (See Note 1.)	T_{VRISE}	–	–	10	ms
Reset time (See Note 2.) (See Note 3.)		T_{RESET}	10	–	–	ms
VDD33 recovery time		$T_{REBOOT33}$	3	–	–	ms
Input signal	Input signal rise time Except CLKI, SCK, SCL, SDA	T_R	–	–	20	ns
	Input signal fall time Except CLKI, SCK, SCL, SDA	T_F			20	

Note 1: Ramp up the power supply within the time shown (from the start until it reaches the minimum valid level as described in *Recommended Operating Conditions*).

Note 2: Only in SPI master mode

Note 3: Conditions: an external capacitor of 2.2 µF connected to LDO18C

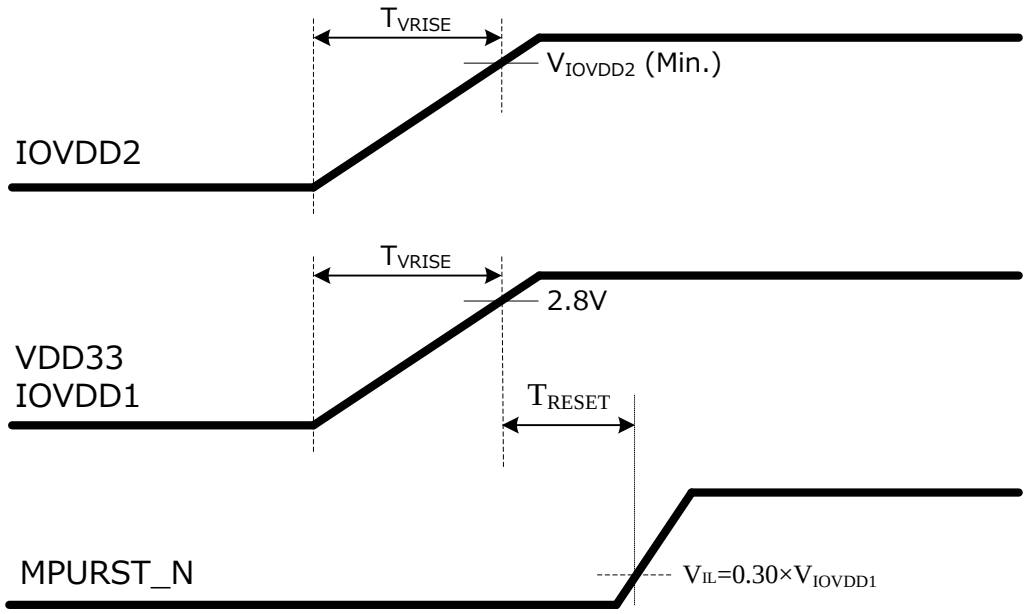


Figure 8-2. Power supply timing requirements.

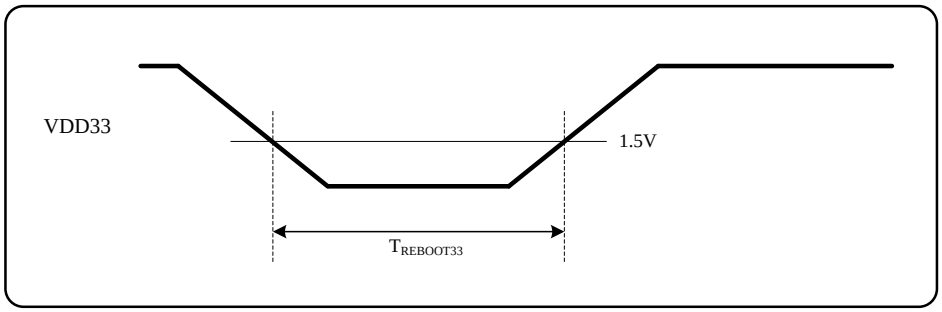


Figure 8-3. VDD33 reboot requirements.

8.5.1.1 Power-on Reset Circuit

Power-on reset logic resets the device on power up, except the embedded microcontroller.
Powering up DVDD18 generates a reset signal to reset 1.8 V core, and powering up DVDD12, a reset signal to reset 1.2 V core. 1.8 V core is reset as well when a VDD33 shutdown is detected by UVLO.

8.5.1.2 Input Signal Rise and Fall Time (except CLKI, SCK, SCL, SDA)

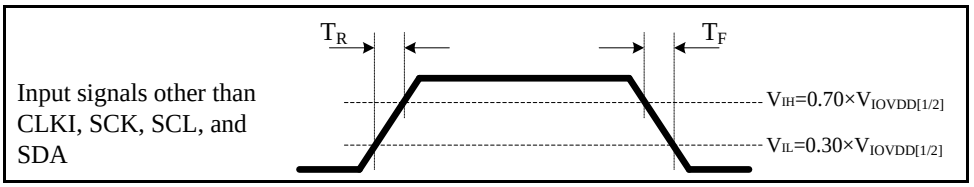


Figure 8-4. Input signal rise and fall timing requirements.

8.5.2 Input Clock (CLKI)

Within the recommended operating conditions

Parameter		Symbol	Min.	Typ.	Max.	Unit
CLKI frequency (See Note 1.)		$1 / T_{FREQ}$	–	24.576	27	MHz
CLKI width	"H" pulse duration	T_{HIGH}	10	–	–	ns
	"L" pulse duration	T_{LOW}	10			
CLKI time	Rise time	T_{RISE}	–	–	30	ns
	Fall time	T_{FALL}			30	
Frequency tolerance		–	–	–	±100	ppm

Note 1:CLKI must be 24.576 MHz when the device is used in SPI master mode.

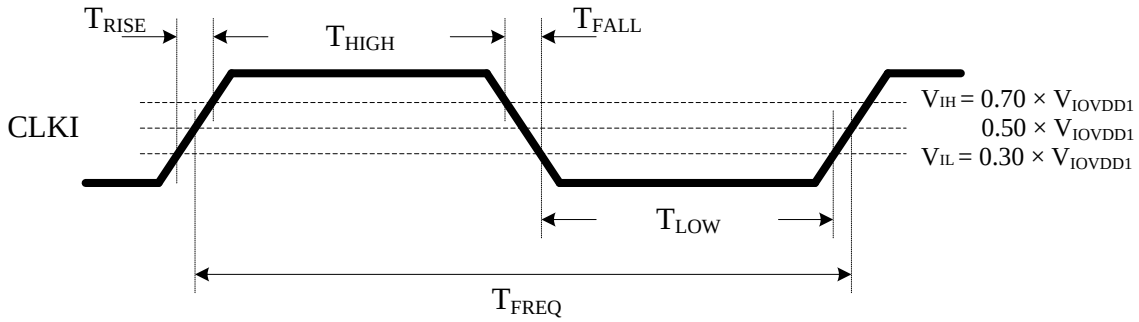


Figure 8-5. CLKI timing requirements.

8.5.3 SPI Timing

The measurement conditions are as follows.

Signal input conditions: V_{IH} = 0.80 × V_{IOVDD1}, V_{IL} = 0.20 × V_{IOVDD1}

Measurement points: V_{IH} = 0.70 × V_{IOVDD1}, V_{IL} = 0.30 × V_{IOVDD1},
V_{OH} = 0.70 × V_{IOVDD1}, V_{OL} = 0.30 × V_{IOVDD1}

8.5.3.1 SPI Master Mode Timing

Capacitive load = 30 pF, and for *Recommended Operating Conditions.*

Parameter		Symbol	Min.	Typ.	Max.	Unit
SCK	Frequency	$1/T_{SCKW}$	–	–	9	MHz
	"H" pulse duration	T_{SCKH}	0.4 × T_{SCKW}	–	0.6 × T_{SCKW}	µs
	"L" pulse duration	T_{SCKL}	0.4 × T_{SCKW}	–	0.6 × T_{SCKW}	
	Output rise and fall time	T_{SCKRF}	10	–	–	ns
MISO	Input setup time	T_{DIS}	30	–	–	ns
	Input hold time	T_{DIH}	10		–	
MOSI	Output delay time	T_{DOV}	–	–	20	ns
	Output hold time	T_{DOH}	−20		–	

MODE 0 is selected when in SPI master mode.

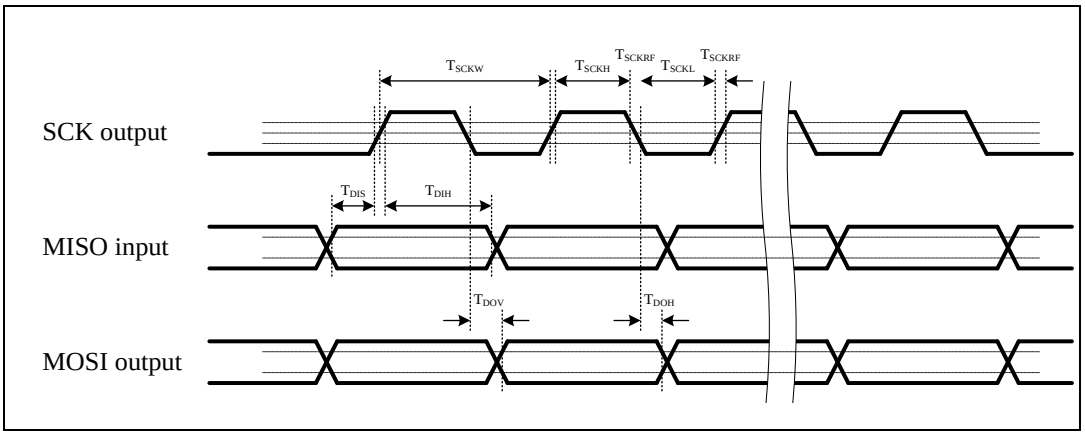


Figure 8-6. SPI master mode timing.

8.5.3.2 SPI Slave Mode Timing

Capacitive load = 30 pF, I_{OH} = −1 mA, I_{OL} = +1 mA, and for *Recommended Operating Conditions*

Parameter		Symbol	Min.	Typ.	Max.	Unit
SCK input frequency		F_{SCK}	–	–	15	MHz
SCK input	"H" duration	T_{CH}	10	–	–	ns
	"L" duration	T_{CL}	10			
	Rise time	T_{CLCH}	–	–	15	ns
	Fall time	T_{CHCL}			15	
SS_N input	Setup time	T_{SSU}	35	–	–	ns
	Hold time	T_{SHD}	10			
MOSI input	Setup time	T_{DSU}	25	–	–	ns
	Hold time	T_{DHD}	10			
SS_N input "H" duration		T_{SW}	20	–	–	ns
MISO output access time		T_{QV}	–	–	30	ns
MISO output data hold time		T_{QX}	2	–	–	ns
MISO output high impedance transition time		T_{QZ}	–	–	20	ns

◆ MOSI Input

Mode 0, Mode 3

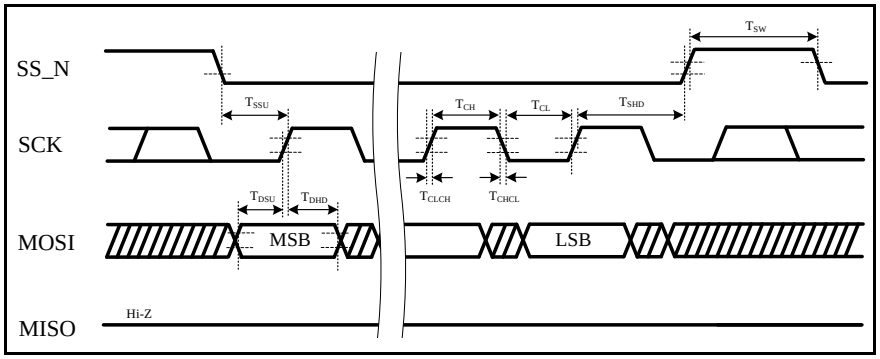


Figure 8-7. MOSI input timing 1.

Mode 1, Mode 2

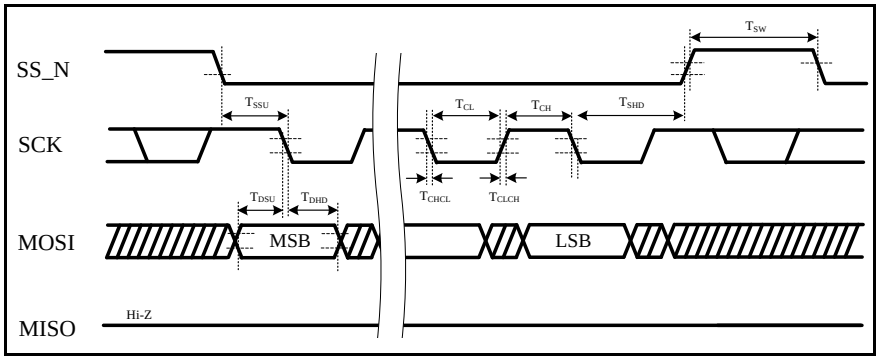


Figure 8-8. MOSI input timing 2.

◆ MISO Output

Mode 0, Mode 3

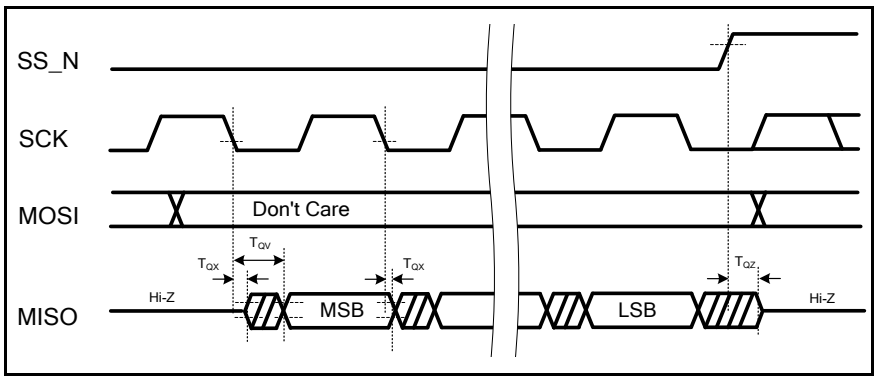


Figure 8-9. MISO output timing 1.

Mode 1, Mode 2

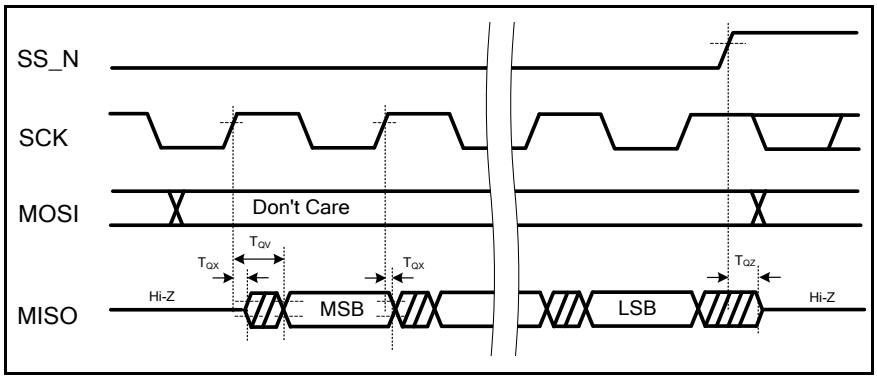


Figure 8-10. MISO output timing 2.

8.5.4 I²C Interface Timing

The measurement conditions are as follows.

Signal input conditions: V_{IH} = 0.80× V_{IOVDD1}, V_{IL} = 0.20 × V_{IOVDD1}

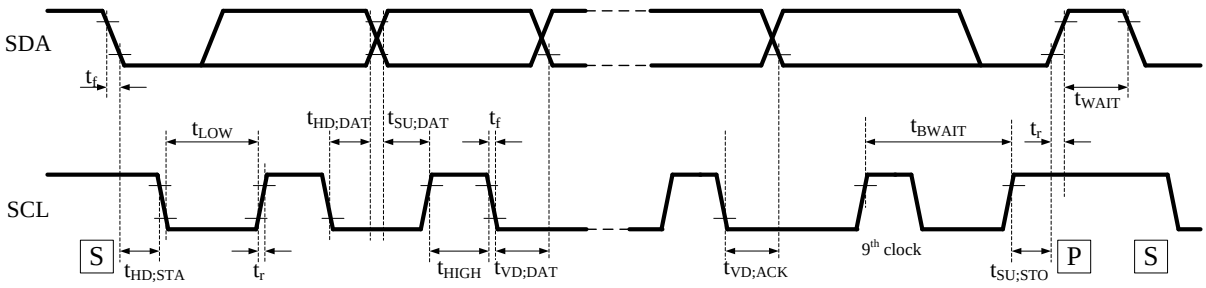
Measurement points: V_{IH} = 0.70× V_{IOVDD1}, V_{IL} = 0.30 × V_{IOVDD1},

V_{OH} = 0.70× V_{IOVDD1}, V_{OL} = 0.30 × V_{IOVDD1}

Assuming operating under *Recommended Operating Conditions.*
CLKI = 24.576 MHz, Capacitive load = 400 pF, I_{OL}= +3.0 mA

Parameter	Symbol	Min.	Typ.	Max.	Unit
SCL input clock frequency	f_{SCL}	0	–	400	kHz
START condition hold time	$t_{HD;STA}$	0.6	–	–	µs
SCL input clock "L" duration	t_{LOW}	1.3	–	–	µs
SCL input clock "H" duration	t_{HIGH}	0.6	–	–	µs
Data input hold time	$t_{HD;DAT}$	0	–	–	µs
Data input setup time	$t_{SU;DAT}$	100	–	–	ns
SDA, SCL input rise time	tr	–	–	300	ns
SDA, SCL input fall time	tf	–	–	300	ns
STOP condition setup time	$t_{SU;STO}$	0.6	–	–	µs
Waiting time from STOP and START conditions	t_{WAIT}	20	–	–	µs
Waiting time between received bytes (See Note 1.)	t_{BWAIT}	20	–	–	µs
Valid data time	$t_{VD;DAT}$	–	–	0.9	µs
Valid data acknowledge time	$t_{VD;ACK}$	–	–	0.9	µs
Each bus line's capacitance load	C_b	–	–	400	pF

Note 1: Wait for more than the specified period of time between the rising edge of the ninth SCL clock and the next when transferring multiple bytes of data.



S: Start Condition, P: Stop Condition

Figure 8-11. I²C timing.

- **YMU836's I²C bus is available only in SPI master mode.**
- **YMU836 acts only as a slave device.**
- **YMU836 does not support high speed mode (Hs mode).**
- **YMU836 does not support repeated start (Sr) and clock stretching.**

8.5.5 Digital Audio Interface Timing

These characteristics are measured under the following conditions.

Signal input conditions: $V_{IH} = 0.80 \times V_{IOVDD[1/2]}$, $V_{IL} = 0.20 \times V_{IOVDD[1/2]}$

Measurement points: $V_{IH} = 0.70 \times V_{IOVDD[1/2]}$, $V_{IL} = 0.30 \times V_{IOVDD[1/2]}$,
$V_{OH} = 0.70 \times V_{IOVDD[1/2]}$, $V_{OL} = 0.30 \times V_{IOVDD[1/2]}$

8.5.5.1 Master Mode

Capacitive load = 30 pF within the recommended operating conditions

Parameter		Symbol	Min.	Typ.	Max.	Unit
SDIN[1/2] input setup time	fs > 48 kHz	T_{SDIS}	16	–	–	ns
	fs ≤ 48 kHz	T_{SDIS}	65			
SDIN[1/2] input hold time	fs > 48 kHz	T_{SDIH}	16	–	–	ns
	fs ≤ 48 kHz	T_{SDIH}	65			
BCLK[1/2] output frequency (See Note 2.)		$1/T_{BCLKW}$	–	64fs 48fs 32fs (See Note 1.)	–	kHz
BCLK [1/2]	Output "H" pulse duration	T_{BCLKHW}	0.35 × T_{BCLKW}	–	–	ns
	Output "L" pulse duration	T_{BCLKLW}	0.35 × T_{BCLKW}			
BCLK[1/2] output rise time, fall time		T_{BCLKRF}	–	–	20	ns
LRCK[1/2] output frequency (See Note 2.)		$1/T_{LRCKW}$	–	fs (See Note 1.)	–	kHz
LRCK[1/2] output delay time		T_{DLRCK}	−50	–	+50	ns
SDOUT[1/2] output delay time		T_{DSDO}	–	–	80	ns

Note 1: fs means a sampling frequency of the digital audio interface.

Note 2: BCLK[1/2] and LRCK[1/2] outputs have timing jitters. The output frequency may fluctuate from the ideal value, depending on CLKI frequency and PLL setting.

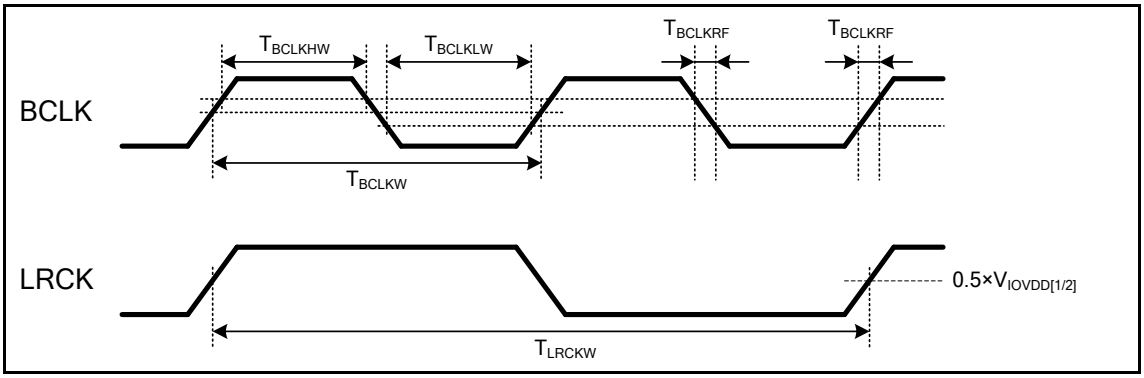


Figure 8-12. Digital audio interface master mode timing.

■ LRCK and SDOUT both change on a BCLK edge

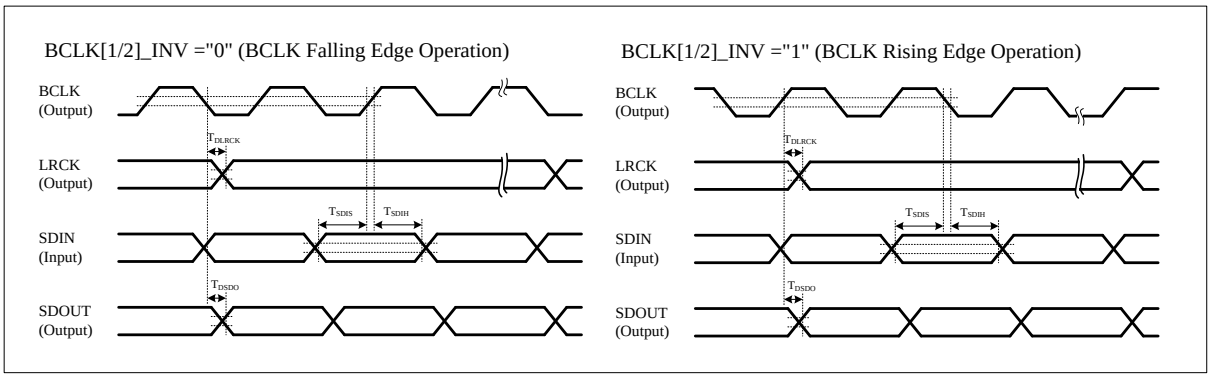


Figure 8-13. Digital audio interface master mode 1 timing.

■ LRCK and SDOUT change on opposite BCLK edges

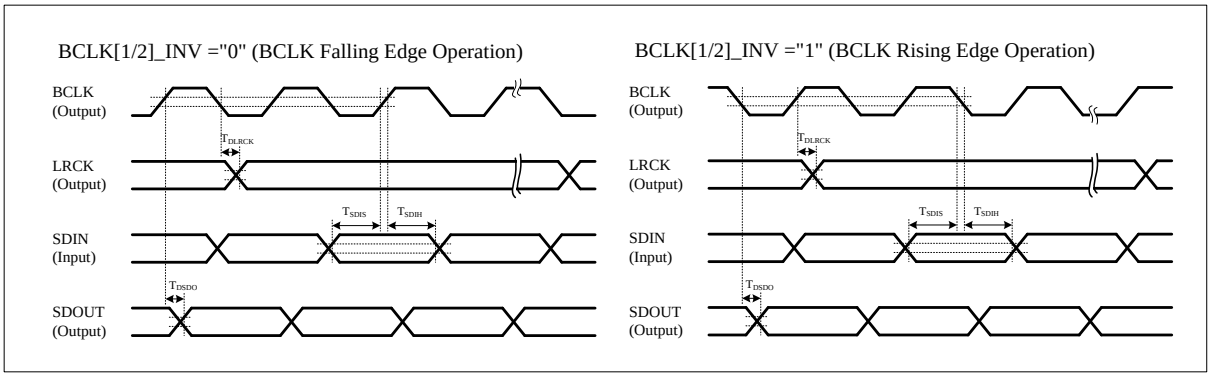


Figure 8-14. Digital audio interface master mode 2 timing.

8.5.5.2 Slave Mode

Capacitive load = 30 pF within the recommended operating conditions

Parameter		Symbol	Min.	Typ.	Max.	Unit
SDIN[1/2] Input setup time	fs > 48 kHz	T_{SDIS}	16	–	–	ns
	fs ≤ 48 kHz	T_{SDIS}	65			
SDIN[1/2] Input hold time	fs > 48 kHz	T_{SDIH}	16	–	–	ns
	fs ≤ 48 kHz	T_{SDIH}	65			
BCLK[1/2] Input frequency		$1/T_{BCLKW}$	–	64fs 48fs 32fs (See Note 1.)	–	kHz
BCLK [1/2]	Input "H" pulse duration	T_{BCLKHW}	0.35 × T_{BCLKW}	–	–	ns
	Input "L" pulse duration	T_{BCLKLW}	0.35 × T_{BCLKW}			
LRCK[1/2] Input frequency		$1/T_{LRCKW}$	–	fs (See Note 1.)	–	kHz
LRCK[1/2] Input setup time	fs > 48 kHz	T_{LRCKS}	16	–	–	ns
	fs ≤ 48 kHz	T_{LRCKS}	65			
LRCK[1/2] Input hold time	fs > 48 kHz	T_{LRCKH}	16	–	–	ns
	fs ≤ 48 kHz	T_{LRCKH}	65			
SDOUT[1/2] Output delay time		T_{DSDO}	–	–	80	ns

Note 1: fs means a sampling frequency of the digital audio interface.

Allowable Input frequency (LRCK frequency) Range
In slave mode, the allowable range of input frequency (LRCK frequency) is predetermined.
Normal playback operation is not always performed when this frequency is not within the range.

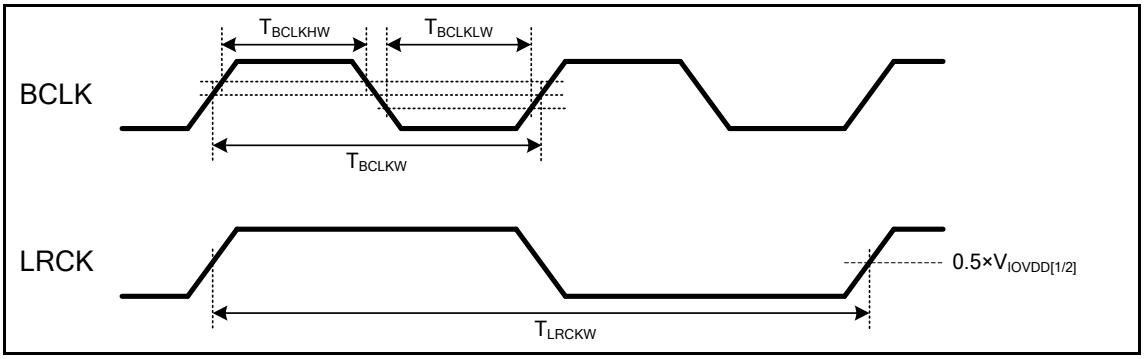


Figure 8-15. Digital audio interface slave mode timing.

■ LRCK and SDOUT both change on a BCLK edge

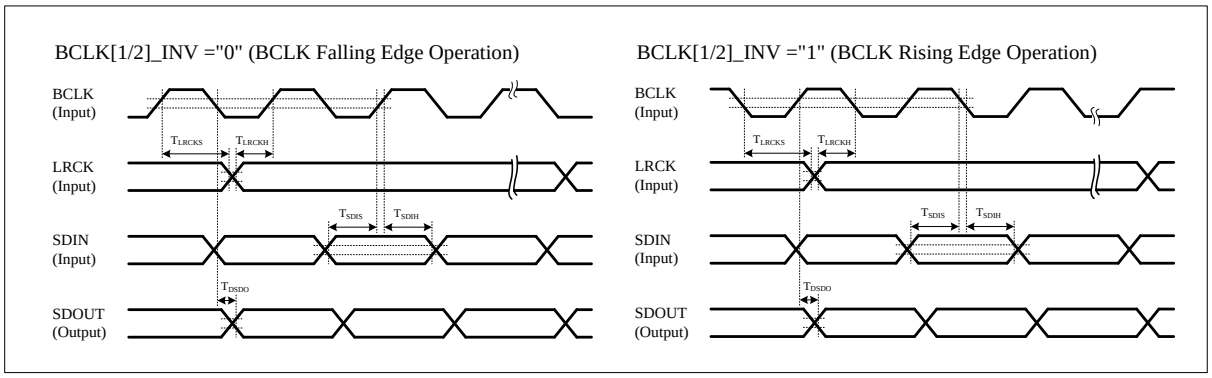


Figure 8-16. Digital audio interface slave mode 1 timing.

■ LRCK and SDOUT change on opposite BCLK edges

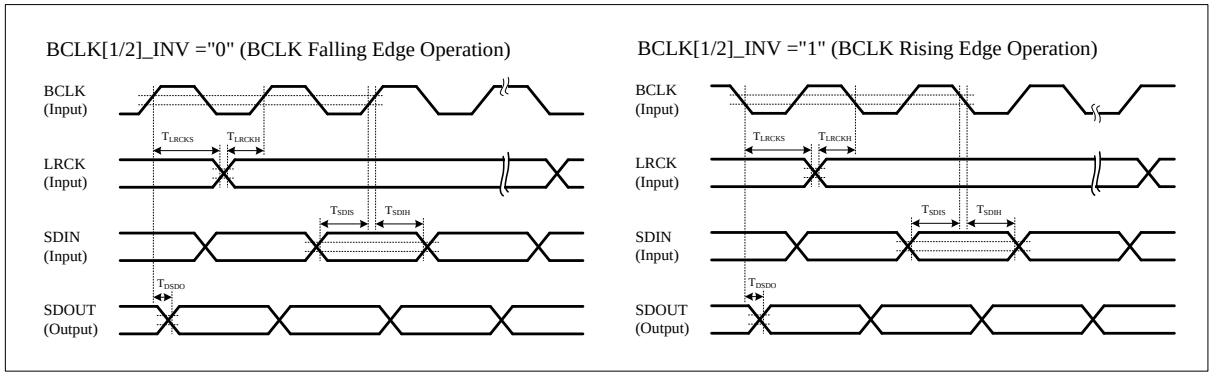


Figure 8-17. Digital audio interface slave mode 2 timing.

8.5.6 PCM Interface Timing

The characteristics are measured under the following conditions:

Signal input conditions: V_{IH} = 0.80 × $V_{IOVDD[1/2]}$, V_{IL} = 0.20 × $V_{IOVDD[1/2]}$

Measurement points: V_{IH} = 0.70 × $V_{IOVDD[1/2]}$, V_{IL} = 0.30 × $V_{IOVDD[1/2]}$,
V_{OH} = 0.70 × $V_{IOVDD[1/2]}$, V_{OL} = 0.30 × $V_{IOVDD[1/2]}$

8.5.6.1 Master Mode

Capacitive load = 30 pF, I_{OH} = −1.0 mA, I_{OL} = +1.0 mA within the recommended operating conditions

Parameter		Symbol	Min.	Typ.	Max.	Unit
SDIN[1/2]	Input setup time	T_{SDIS}	40	–	–	ns
	Input hold time	T_{SDIH}	40			ns
BCLK[1/2] Output frequency (See Note 4.)		$1/T_{BCLKW}$	–	512fs (See Note 2.) 256fs (See Note 3.) 192fs 128fs 96fs 64fs 48fs 32fs 24fs 16fs 8fs (See Note 1.)	–	kHz
BCLK [1/2]	Output "H" pulse duration	T_{BCLKHW}	0.35 × T_{BCLKW}	–	–	ns
	Output "L" pulse duration	T_{BCLKLW}	0.35 × T_{BCLKW}			ns
BCLK[1/2] Output rise, fall time		T_{BCLKRF}	–	–	20	ns
LRCK[1/2] Output frequency (See Note 4.)		$1/T_{LRCKW}$	–	fs (See Note 1.)	–	kHz
LRCK[1/2] Output delay time		T_{DLRCK}	−65	–	0	ns
LRCK[1/2] Output rise, fall time		T_{LRCKRF}	–	–	20	ns
SDOUT[1/2] Output delay time	First one bit of slot 0	T_{D0SDO}	–	–	80	ns
	Bits other than the above	T_{D1SDO}			80	
SDOUT[1/2] High impedance transition time		T_{DZSDO}	0	–	60	ns

Note 1: fs means a sampling frequency of PCM interface.

Note 2: Only when the sampling frequency of the 8 kHz can be setting.

Note 3: Only when the sampling frequency of the 8 kHz and 16 kHz can be setting.

Note 4: BCLK[1/2] and LRCK[1/2] outputs have timing jitters. The output frequency may different from the ideal frequency depending on CLKI frequency and PLL setting.

■ BCLK

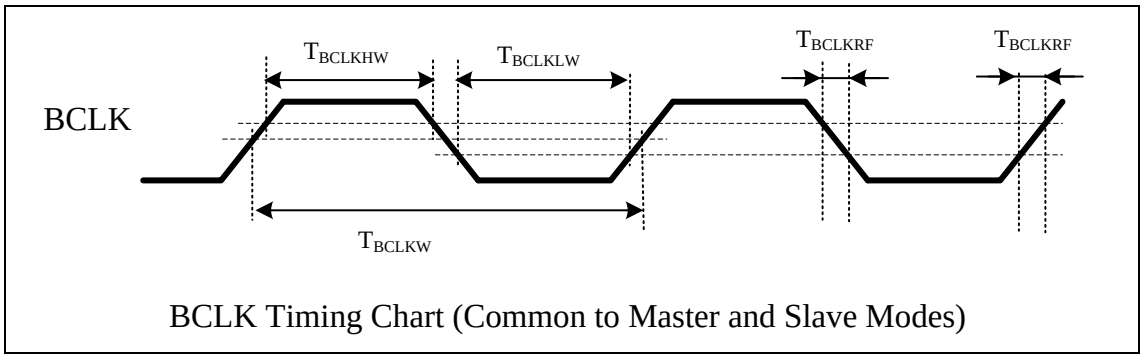


Figure 8-18. PCM interface master mode (BCLK) timing.

■ LRCK

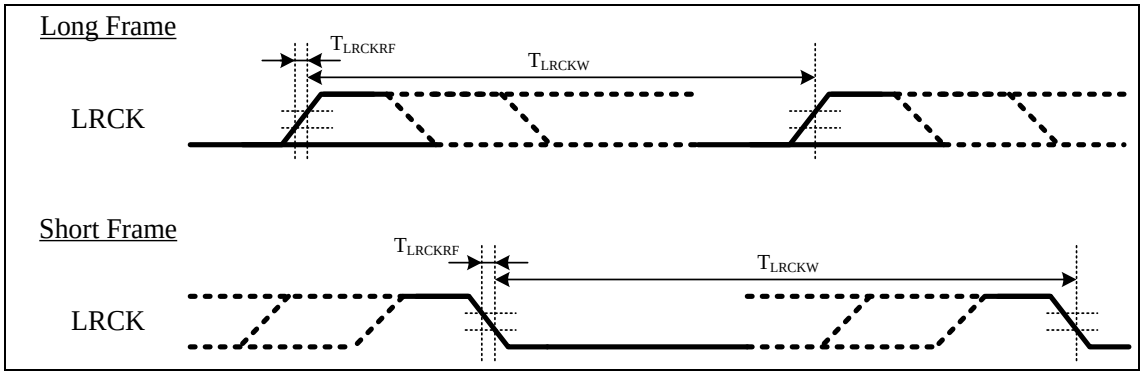


Figure 8-19. PCM interface master mode (LRCK) timing.

■ Long Frame Operation

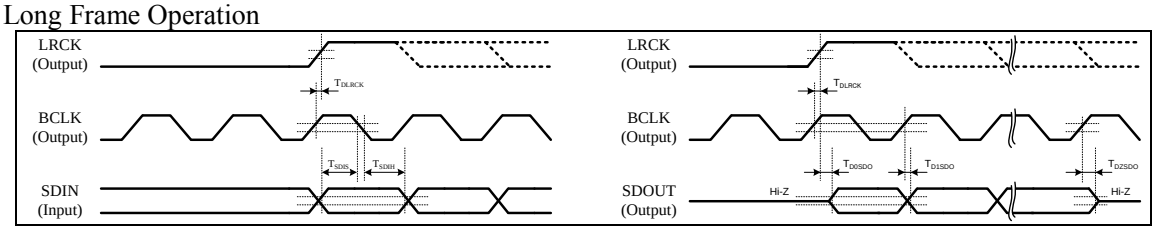


Figure 8-20. PCM interface master mode (Long Frame) timing.

■ Short Frame Operation

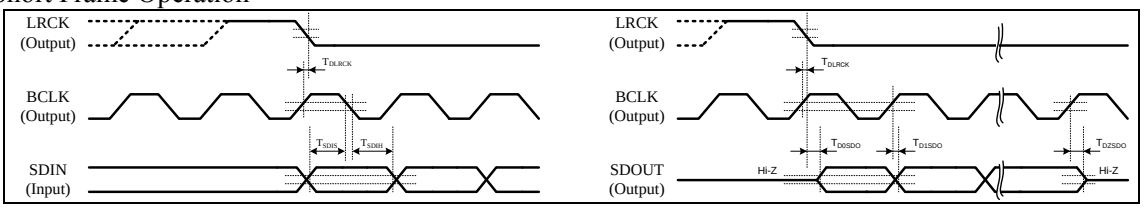


Figure 8-21. PCM interface master mode (Short Frame) timing.

8.5.6.2 Slave Mode

Capacitive load = 30 pF, I_{OH} = −1.0 mA, I_{OL} = +1.0 mA within the recommended operating conditions

Parameter		Symbol	Min.	Typ.	Max.	Unit
SDIN[1/2]	Input setup time	T_{SDIS}	40	–	–	ns
	Input hold time	T_{SDIH}	40			ns
BCLK[1/2] Input frequency		$1/T_{BCLKW}$	–	8fs to 512fs (See Note 1.)	–	kHz
BCLK[1/2]	Input "H" pulse duration	T_{BCLKHW}	0.35 × T_{BCLKW}	–	–	ns
	Input "L" pulse duration	T_{BCLKLW}	0.35 × T_{BCLKW}			ns
LRCK[1/2] Input frequency		$1/T_{LRCKW}$	–	fs (See Note 1.)	–	kHz
LRCK[1/2] Input setup time		T_{LRCKS}	35	–	0.75 × T_{BCLKW}	ns
LRCK[1/2] Input "H" pulse duration		$T_{LRCKW}/2$	T_{BCLKW}	–	–	ns
SDOUT[1/2] Output delay time	First one bit of slot 0	T_{D0SDO}	–	–	80	ns
	Bits other than the above	T_{D1SDO}			80	
SDOUT[1/2] High impedance transition time		T_{DZSDO}	0	–	60	ns

Note 1: fs means a sampling frequency of PCM interface.

⚠ Supported Input frequency (LRCK frequency) Range
Slave mode input clock (LRCK) must be in the supported frequency range.
Normal playback operation is not always performed when this frequency is not within the range.

■ Long Frame Operation

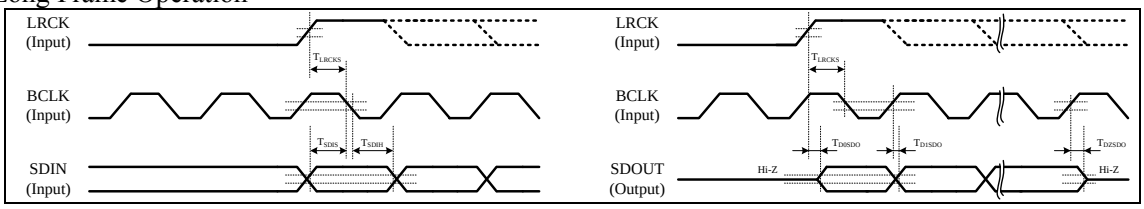


Figure 8-22. PCM interface slave mode (Long Frame) timing.

■ Short Frame Operation

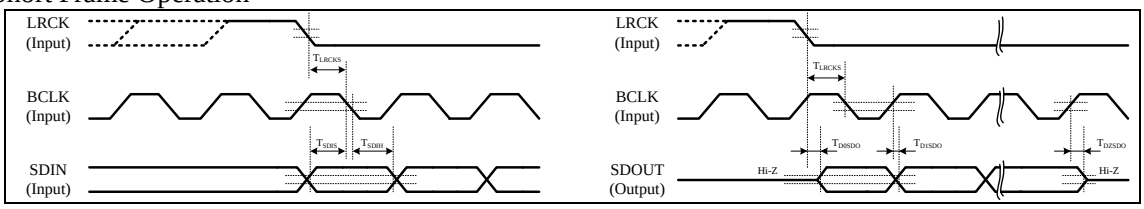


Figure 8-23. PCM interface slave mode (Short Frame) timing.

8.5.7 Digital Microphone Interface Timing

These characteristics are measured under the following conditions:

Signal input conditions: V_{IH} = 0.80 × V_{IOVDD1}, V_{IL} = 0.20 × V_{IOVDD1}

Measurement points: V_{IH} = 0.70 × V_{IOVDD1}, V_{IL} = 0.30 × V_{IOVDD1},
V_{OH} = 0.70 × V_{IOVDD1}, V_{OL} = 0.30 × V_{IOVDD1}

Capacitive load = 30 pF within the recommended operating conditions

Parameter		Symbol	Min.	Typ.	Max.	Unit
DMCK output frequency		$1/T_{DMCKW}$	–	128fs 64fs 32fs (See Note 1.)	–	kHz
DMCK	Output "H" pulse duration	T_{DMCKHW}	60	–	–	ns
	Output "L" pulse duration	T_{DMCKLW}	60			
DMCK output rise time, fall time		T_{DMCKRF}	–	–	20	ns
DMDIN[0/1]	Input setup time	T_{DMDIS}	50	–	–	ns
	Input hold time	T_{DMDIH}	15			

Note 1: fs means a sampling frequency of the digital microphone interface.
This sampling frequency of 48 kHz may fluctuate from the ideal value, depending on CLKI frequency and PLL setting.

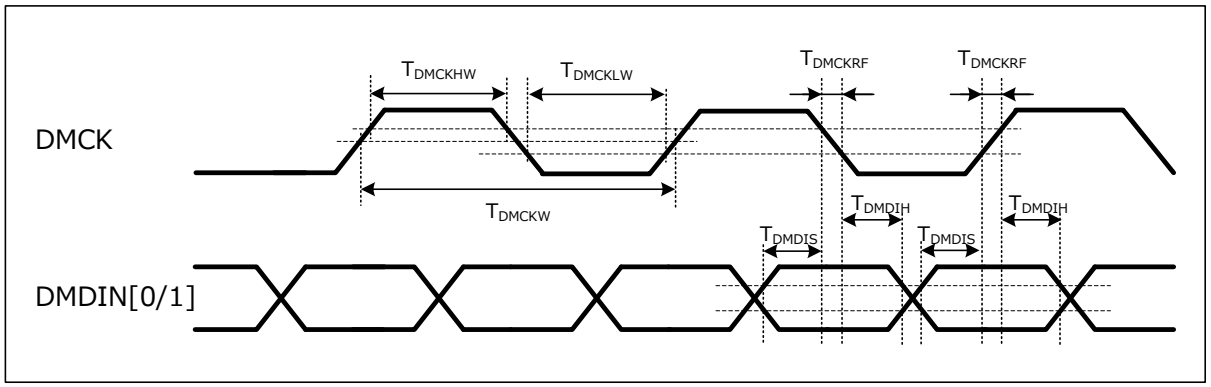


Figure 8-24. Digital microphone interface timing.

8.6 Analog Characteristic

Unless otherwise noted, T_a = 25°C, V_{VDD33} = $V_{IOVDD[1/2]}$ = 3.30 V.

8.6.1 Line Output Amplifier

DAC to LINEOUT, R_L = 20 kΩ

Parameter	Description	Min.	Typ.	Max.	Unit
Fixed gain	Line Output Amplifier	–	0	–	dB
Line output load	R_L	8k	–	–	Ω
Maximum output voltage amplitude		–	1	–	V_{rms}
THD+N	f = 1 kHz, 600 mV_{rms}	–	0.01	–	%
Noise floor	no input, A-weighted, LO[1/2]VOL_L/R = 0dB	–	−100	–	dBV
	no input, A-weighted, LO[1/2]VOL_L/R = −36dB		−109		
Crosstalk	1 kHz	–	−105	–	dB
PSRR	VDD33, f = 217 Hz	–	97	–	dB
Reference voltage		–	0	–	V
Output offset Voltage	LO[1/2]VOL_L/R = −36dB	–	0.1	–	mV
Output impedance		–	100	–	Ω

8.6.2 MIC Amplifiers #1 to #3

MIC to ADC, MC[1/2/3]VOL = 0 dB

Parameter	Description	Min.	Typ.	Max.	Unit
THD+N	f = 1 kHz	–	0.01	–	%
Noise Floor	No input, A-weighted	–	-93.5	–	dBFS
Input impedance	Differential	–	10k	–	Ω
	Single-ended		12.8k		

8.6.3 MIC Amplifiers #4

MIC to ADC, MC4VOL = 0 dB

Parameter	Description	Min.	Typ.	Max.	Unit
THD+N	f = 1 kHz	–	0.01	–	%
Noise Floor	No input, A-weighted	–	-93.5	–	dBFS
Input impedance		–	12.8k	–	Ω

8.6.4 VREF

Parameter	Description	Min.	Typ.	Max.	Unit
VREF Voltage		–	0.9	–	V

8.6.5 MIC Biases #1 to #3

Parameter	Description	Min.	Typ.	Max.	Unit
Output voltage		–	1.8 2.0 2.7	–	V
Output current		–	–	1.4	mA
Noise level	A-weighted	–	−105	–	dBV

8.6.6 ADC

Parameter	Description	Min.	Typ.	Max.	Unit
Resolution		–	24	–	bit
Full scale input voltage		–	1	–	V_{rms}

8.6.7 DAC

Parameter	Description	Min.	Typ.	Max.	Unit
Resolution		–	24	–	bit
Full scale input voltage		–	1	–	V_{rms}

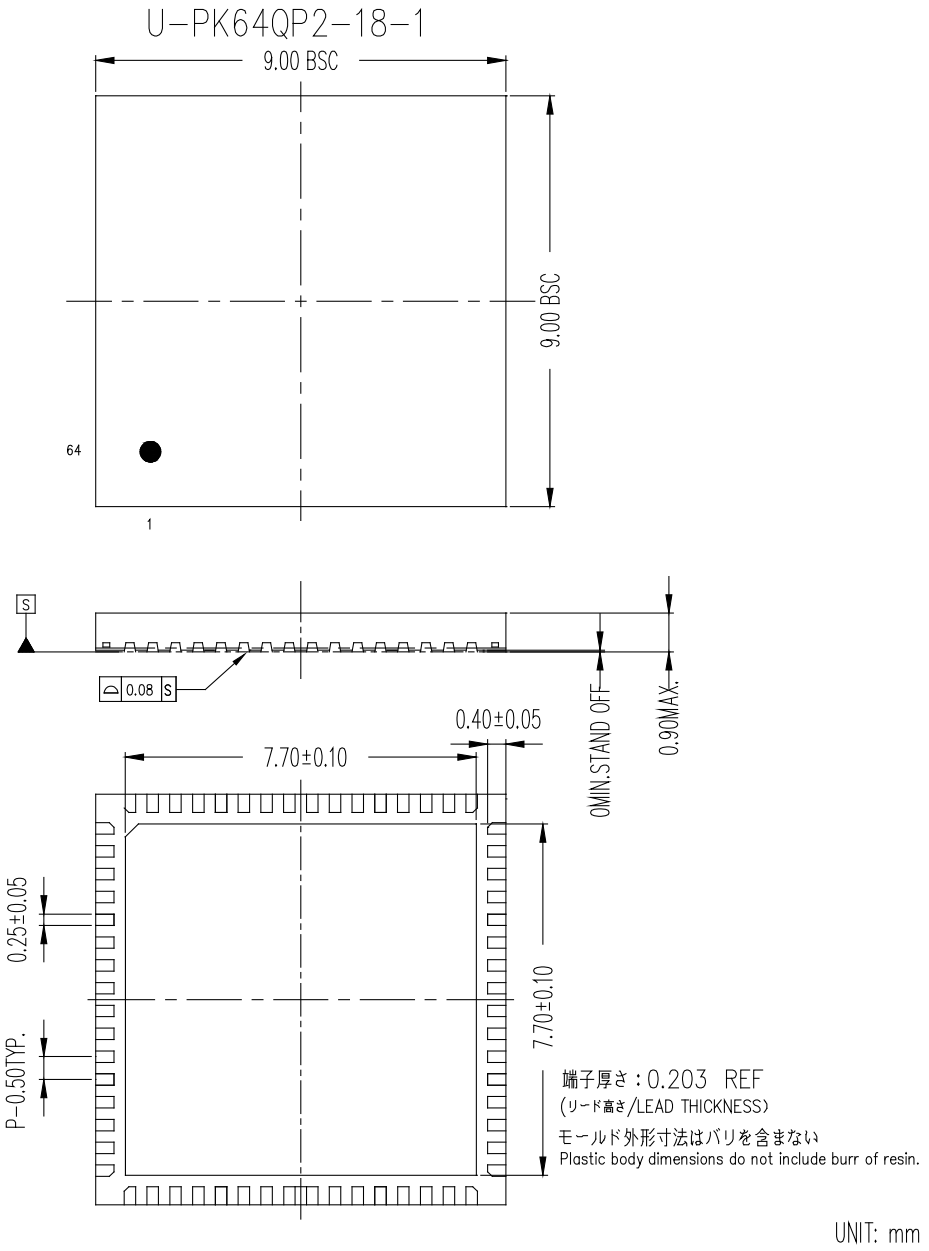
8.6.8 LINEOUT1/LINEOUT2 Volume (LO[1/2]VOL_L/R)

Parameter	Description	Min.	Typ.	Max.	Unit
Volume setting range		−36	–	0	dB
Volume step width		–	0.25 0.5 1	–	dB
Mute attenuation		80	–	–	dB

8.6.9 MIC1/MIC2/MIC3/MIC4 Gain Settings (MC[1/2/3/4]VOL)

Parameter	Description	Min.	Typ.	Max.	Unit
Volume setting range		−30	–	+30	dB
Volume step width		–	0.5 1 2	–	dB
Mute attenuation		80	–	–	dB

9 Package Dimensions



注） 1. 表面実装LSIは、保管条件、および、半田付けについての特別な配慮が必要です。
2. 組立工場により、寸法や形状などが異なる場合があります。
詳しくはヤマハ代理店までお問い合わせください。

Note: 1. Special attention needs to be paid to the storage conditions and soldering method of the surface mount IC.
2. Dimension, form, etc. may differ depending on assembly plants.
For details, please contact your local Yamaha agent.

10 Peripheral Circuit Example

10.1 SPI Master Mode

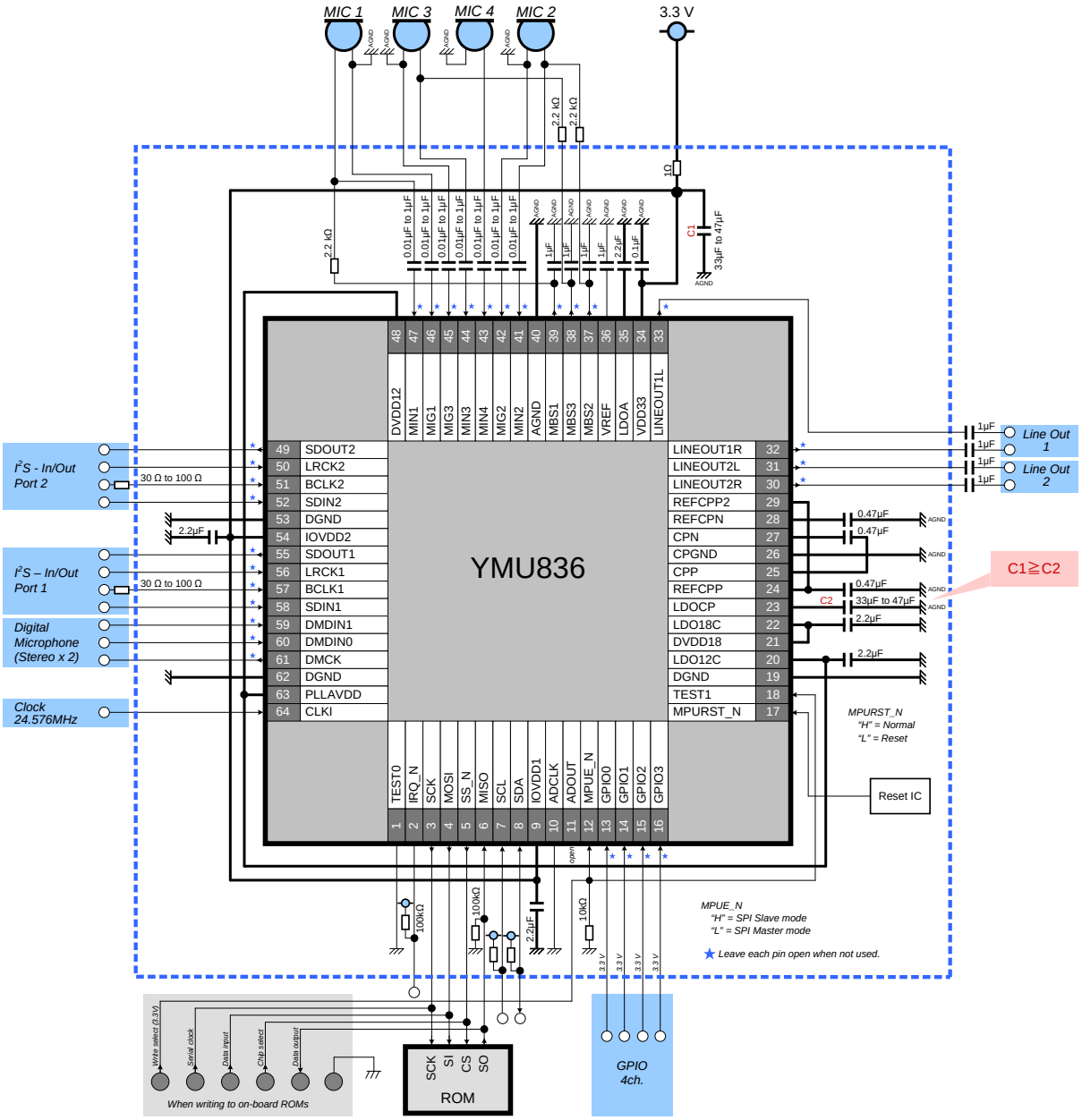


Figure 10-1. Application example (Master).

10.2 SPI Slave Mode

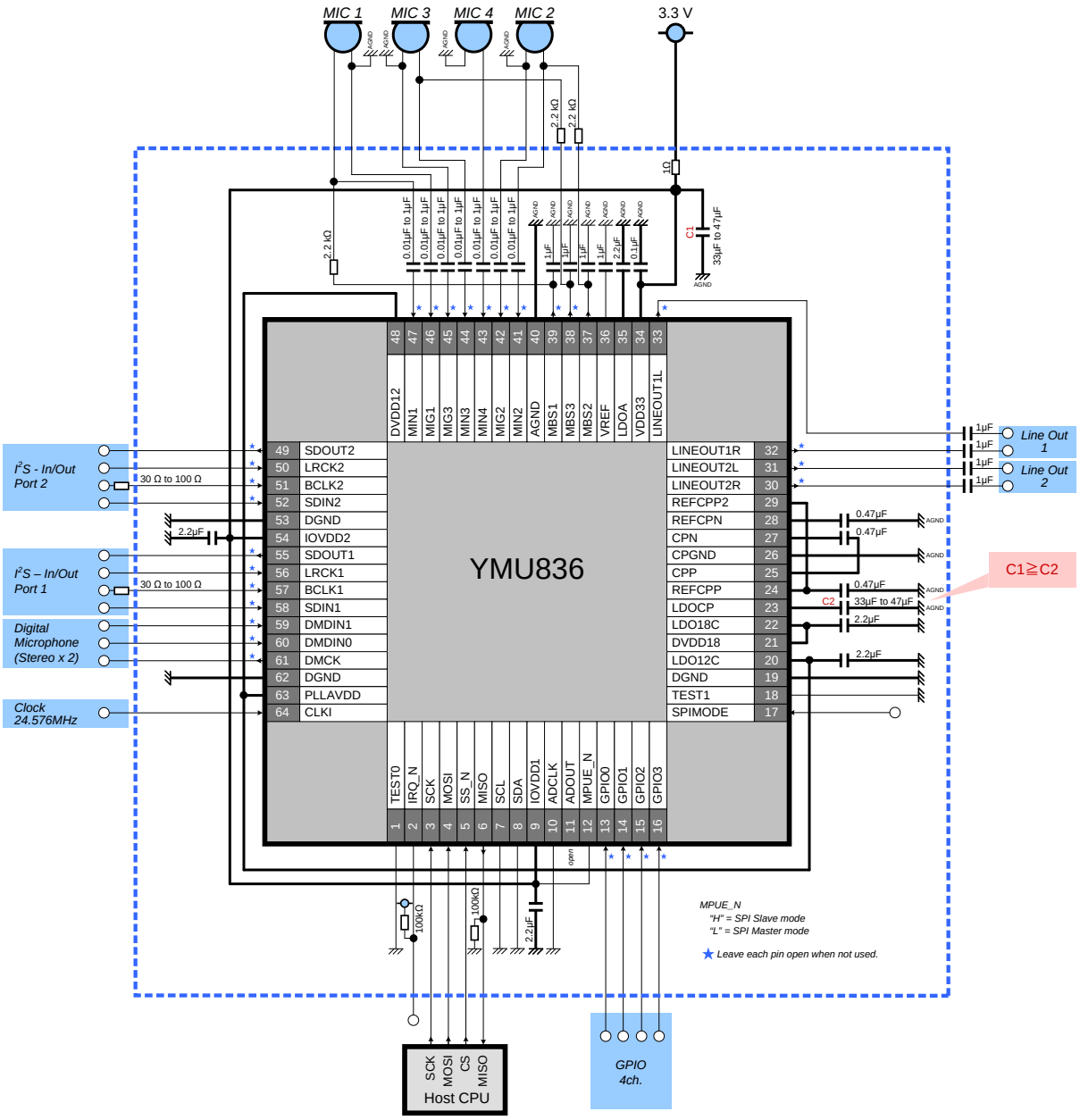


Figure 10-2. Application example (Slave).

● Input Impedance (R_M)

・Single-ended Input Pins

Table 10.1. Input Impedance (Single-ended Input Pins)

Pre-Amplifier Gain [dB] : Input Impedance [Ω]											
+30.0	12.2k	+19	11.4k	+8	15.0k	−3	12.0k	−14	10.9k	−25	10.2k
+28.0	12.2k	+18	11.4k	+7	15.0k	−4	12.0k	−15	10.6k	−26	10.2k
+26.0	12.0k	+17	10.8k	+6	15.0k	−5	12.0k	−16	10.6k	−27	10.2k
+24.0	11.9k	+16	10.8k	+5	13.9k	−6	12.0k	−17	10.6k	−28	10.2k
+23.5	11.9k	+15	10.8k	+4	13.9k	−7	11.4k	−18	10.6k	−29	10.2k
+23.0	11.8k	+14	10.8k	+3	13.9k	−8	11.4k	−19	10.4k	−30	10.2k
+22.5	11.8k	+13	10.2k	+2	13.9k	−9	11.4k	−20	10.4k		
+22.0	11.8k	+12	10.2k	+1	12.8k	−10	11.4k	−21	10.4k		
+21.5	11.7k	+11	10.2k	0	12.8k	−11	10.9k	−22	10.4k		
+21.0	11.4k	+10	10.2k	−1	12.8k	−12	10.9k	−23	10.2k		
+20.0	11.4k	+9	15.0k	−2	12.8k	−13	10.9k	−24	10.2k		

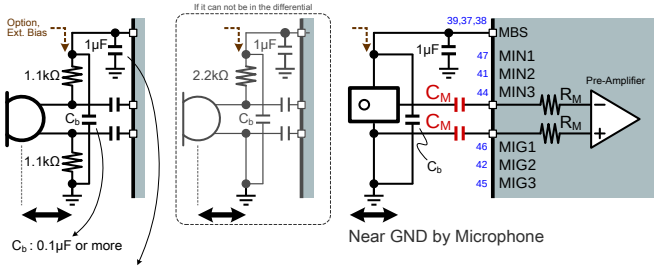
・Differential Input Pins

Table 10.2. Input Impedance (Differential Input Pins)

Pre-Amplifier Gain [dB] :	Input Impedance [Ω]
−30 to +30	10.0k

● MIC1, MIC2, MIC3

Differential Input Configuration

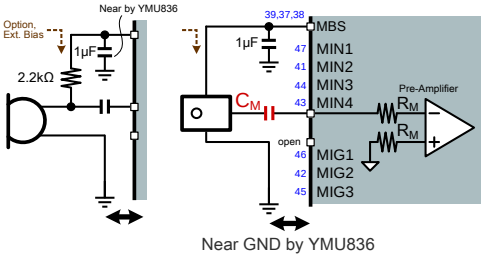


Near by YMU836, use the capacitor bypassing when the signal trace:

1. goes through noisy areas of PCB,
2. is long, or
3. goes through flexible PCB.

● MIC1, MIC2, MIC3

Single-ended Input Configuration



$$C_M = 0.01[\mu F] \cdots 1.0[\mu F]$$

$$f_C = \frac{1}{2\pi \times R_M \times C_M}[Hz]$$

SHARING PASSION & PERFORMANCE

Notice All specifications are subject to change for product improvement without notice.

AGENT

YAMAHA CORPORATION

Address Inquiries to :
Semiconductor Sales & Marketing Department

■Head Office 203, Matsunokijima, Iwata,
Shizuoka, 438-0192, Japan
Tel. +81-539-62-4918 Fax.+81-539-62-5054

■Tokyo Office 2-17-11, Takanawa, Minato-ku,
Tokyo, 108-8586, Japan
Tel. +81-3-5488-5431 Fax.+81-3-5488-5088

Printed in Japan